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Final Report

DEVELOPMENT OF A LOW-COST MEDIUM-SPEED MASS RANDOM-ACCESS MEMORY

C. Chong
R. Mosenkis
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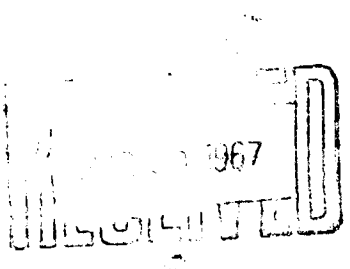
Univac Division, Sperry Rand Corp.

TECHNICAL REPORT NO. RADC-TR-66-814
January 1967



Rome Air Development Center
Research and Technology Division
Air Force Systems Command
Griffiss Air Force Base, New York

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AFLC, GAFB, N.Y., 7 Mar 67-143

FOREWORD

This final technical report was prepared by C. Chong, R. Mosenkis, and D. K. Hanson of Univac Division, Sperry Rand Corporation, Univac Engineering Center, Blue Bell, Pa., under contract AF 30(602)-3825, Project 5581. The RADC project engineer was Mr. Robert F. Long, EMIIO-1.

The work, covered by this report, was accomplished during the period 30 June 1965 through 1 October 1966.

This document contains information embargoed from release to Sino-Soviet Bloc Countries by AFR 400-10, "Strategic Trade Control Program."

Mr. W. Bartik, Director, Defense Research and Development, Philadelphia, provided technical guidance and general management of the contract. Messrs G. Reid, A. Schultz, R. Mosenkis, and D. K. Hanson participated in the research and cooperated in writing this report.

This report has been reviewed and is approved.

Approved: FRANK J. TOMAINI
Chief, Information Processing Branch

Approved: JAMES J. DIMEL, Colonel, USAF
Chief, Intel and Info Processing Division

FOR THE COMMANDER: IRVING J. GABELMAN
Chief, Advanced Studies Group

ABSTRACT

The concept of a nonmechanical, mass, random access, plated-wire memory has been validated in this phase of the continuing U. S. Air Force program. The memory model fabricated for this contract has 10^7-bit positions housing over 2.3 megabits of plated wire. Of these bits, 32,768 4-bit words have been exercised with a memory exerciser. The following characteristics of the plated-wire mass memory have been demonstrated:

Nondestructive readout (NDRO),

Selection in the bit dimension to minimize electronics costs,

Simple mechanical plane configuration,

Random access,

Electrical alterability.

The final test of the plane revealed some defective areas which resulted from the large surface area. Making a smaller plane would easily eliminate this condition.

All the objectives of the program have been achieved, including the projected production cost of less than $0.01 per bit. The contractor feels that as a result of this program, the building of a mass (10^8-bit), random access, plated-wire memory is economically feasible and well within the state-of-the-art.

CONTENTS

ILLUSTRATIONS

EVALUATION

1. Contract AF30(602)-3825 for the Development of a Medium-Speed Mass Random-Access Memory was successfully completed by Univac Division of Sperry Rand Corporation. A working feasibility model of the plated wire memory was demonstrated at the Univac plant in Blue Bell, Pennsylvania. The model contained 2.3 million bits, approximately 131,000 of which were accessible by electronics.

2. The operation of this feasibility model represents a milestone in the development of solid-state militarized mass memories. Many command and control data processing systems now in development will operate in an adverse environment, including temperature extremes, high humidity, shock, and vibration. No foreseeable moving media type of memory will be suitable for use in this environment. Both EMIIO engineers and Univac feel that as a result of this program, the building of a militarized 10^8 bit plated wire random-access memory is economically feasible and well within the state-of-the-art. Thus, the Air Force's capability will be proportionately enhanced as these memories are used with future Air Force data processing systems.

3. The subject contract complements a continuing program in the exploratory development of computer techniques and devices for computer memories. User requirements range from small capacity, ultra high-speed memories to extremely large capacity bulk storage devices. The Univac plated-wire effort is aimed to goals in the middle region of the hierarchy of storage. The results of this effort will be brought to the attention of all potential users and recommended for future systems.

George E. Grindall

GEORGE E. GRINDALL, Lt., USAF
Sys Infor Sciences Section

SECTION 1

INTRODUCTION

1-1. GENERAL

This volume is the final report on work performed under contract AF 30(602)3825 during the period 30 June 1965 through 1 October, 1966. The objective of the continuing program was to develop a low-cost, medium-speed, mass, random-access, plated-wire memory. The memory was to possess the following characteristics as a minimum goal:

Capacity expandable to 10^8 bits.

Production cost of a 10^8-bit memory of less than $0.01 per bit.

Random-access cycle time of 50 microseconds or less.

Nonvolatile, nonmechanical, electrically alterable, bi-stable storage.

Physical dimensions permitting construction of a complete 10^8-bit memory in a volume of no more than 30 cubic feet.

The Univac Division employed magnetic plated wire as the basic memory element. Plated wire was chosen for low cost and for other characteristics suitable for such an application. The feasibility of a plated-wire mass memory was demonstrated under a study contract AF 30(602)3430. The study indicated that such a memory would have the listed requirements, along with the following improved characteristics:

Potential production cost of $0.001 to $0.005 per bit.

Random-access cycle time as low as 1 microsecond.

Projected volume of 20 cubic feet for a 10^8-bit memory.

The objective of contract AF 30(602)3825 was to further the program by developing and building a breadboard memory that houses at least one

million storage bits, of which at least one hundred thousand are exercised. The basic module is 10^7 bits, ten of which are used to make a 10^8-bit memory.

1-2. SUMMARY OF PROGRESS

The project was divided into three phases, each approximately of a 4-month duration. During Phase I, experimental and theoretical investigations were conducted to determine word-line configuration, width, and spacing; bit-line spacing; and memory-plane design. During Phase II, the memory model was constructed. At the same time, a memory exerciser was designed, built, and tested. During Phase III, the memory model was tested.

1-3. REPORT ORGANIZATION

Section II of this final report describes the plated-wire, the memory system, and the packaging and construction of the memory.

Section III gives a description of the word line and bit line configuration including the final parameters selected for each configuration.

Section IV describes the memory model.

Section V details the memory circuits.

Section VI contains the description of the memory exerciser.

Section VII comprises the final test results.

Section VIII gives the conclusions and recommendations based on the results of the work completed.

SECTION II

MEMORY SYSTEM

2-1. THE PLATED-WIRE MEMORY ELEMENT

The memory element consists of a wire substrate made of beryllium-copper drawn to a 0.005-inch diameter and electroplated with a magnetic thin film. The magnetic film is the same 81-percent-nickel, 19-percent-iron alloy widely used in planar thin-film memory elements. The coating is continuous and is plated in the presence of a circumferential magnetic field that establishes a magnetic anisotropy axis, or preferred magnetization direction, circumferentially around the wire. Figure 1 is a simplified diagram of the plating apparatus and the electrical test that provides immediate control of the process. The magnetic material is electroplated on a continuously moving wire in room environment. The continuously moving wire is electrically tested with a complete operating memory pulse program.

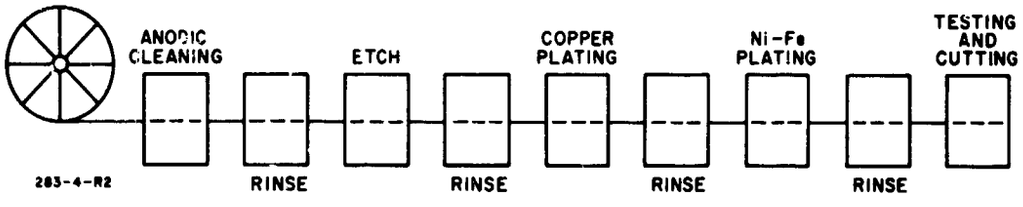

Figure 1. Wire Plater and Tester

Information is stored according to the sense of the circumferential magnetization in the portion of the plated wire encircled by the word strap; clockwise magnetization represents a stored 1; counterclockwise magnetization represents a stored 0. Figure 2 shows a sketch of the plated wire and the word drive line which forms a one-turn solenoid encircling many plated wires (only one is shown). To read the stored information, a word current is applied to the word strap which encircles the plated wire at right angles.

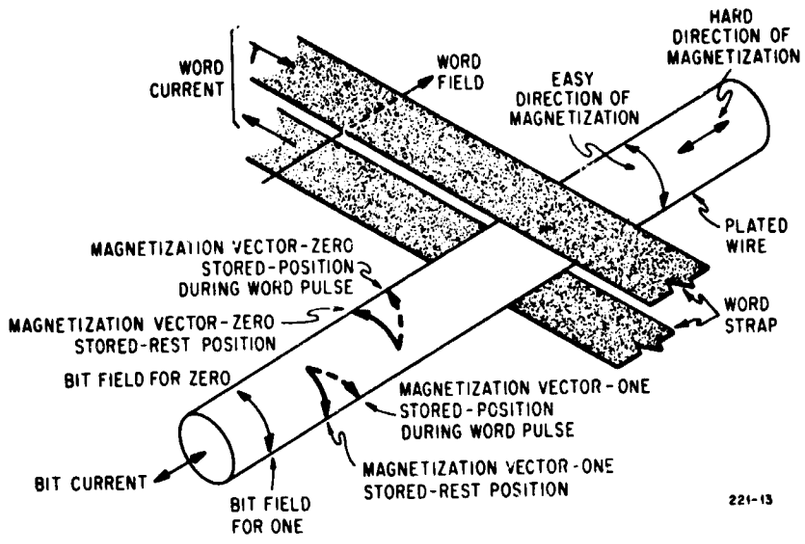

Figure 2. Information Storage on Plated Wire

The word current produces a word field along the axis of the wire. This word field tilts the magnetization vector from its circumferential rest position towards the axis of the wire. The resulting flux change causes a voltage change (sensed at the ends of the plated wire) of a certain polarity for a stored 1 and of the opposite polarity for a stored 0. Figure 3 shows a qualitative vector diagram of the magnetization vector position. The amplitude of the word current is controlled so that when the current is turned off the magnetization vector returns to its original rest position under the influence of the anisotropy and demagnetizing fields; thus, the readout is nondestructive.

Information is written into the wire by the time coincidence of the word current and a steering-bit current through the plated wire. When the bit current flows in one direction, the magnetization vector is so steered that, when the bit and word current end, the vector is in the 1 (rest) position; when the bit current flows in the other direction, the magnetization vector is left in the 0 position.

Operating parameters of the plated wire for the memory are as follows:

Word-strap width:	33 mils, 1/2 turn*, on 45-mil centers.
Word current:	1 ampere.

* One-half-turn line denotes a word line consisting of a top strap over a ground plane.

Bit current:	±32 milliamperes.
Output voltage:	±10 millivolts nominal, 5 millivolts worst-case with off-nominal currents.
Switching time:	80 nanoseconds (for a 40-nanosecond fall time word current).

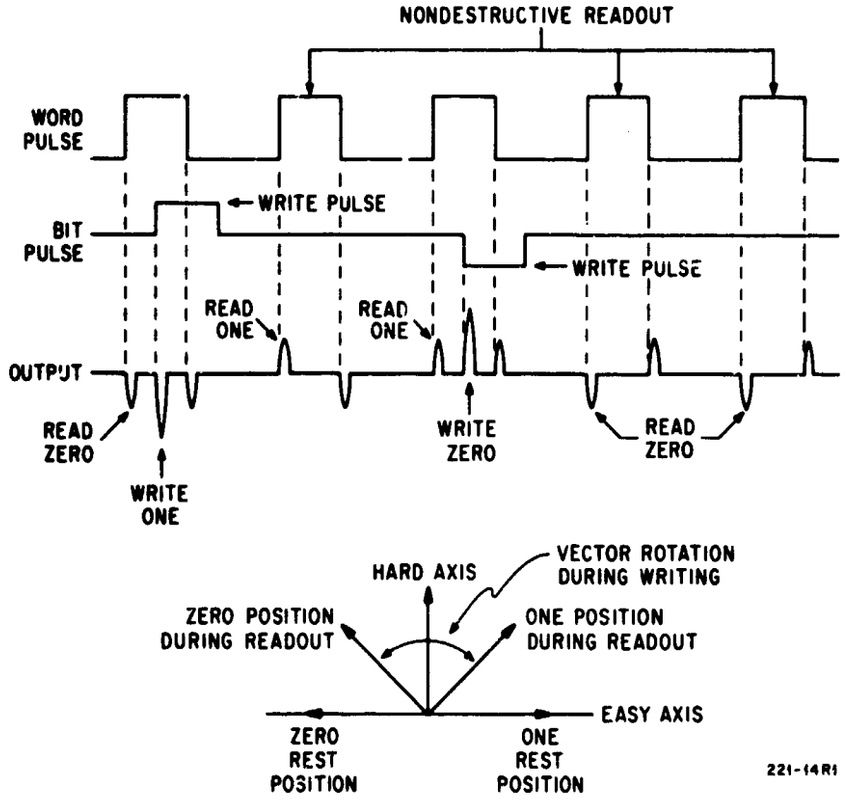

Figure 3. Read and Write Operations

It is important to note that the word-drive current used for reading is of the same amplitude as that used for writing. The word-drive current in the drive line must not adversely affect the information stored in the non-selected words. Similarly, the bit-write current that flows in the plated wires must control the magnetization direction in only the one selected bit.

The magnetic plating is continuous and, if more than 20 to 25 bits per inch along the wire are used, there is a tendency for interference between bits. This interference is reversible. If 0 is written millions of times on each side of a 1, with the program shown in Figure 3, the signal read from the 1 will be diminished. If 1 is written on each side of the center

test bit, the signal read from the test bit will be increased. This effect is eliminated by the use of the writing technique shown in Figure 4.

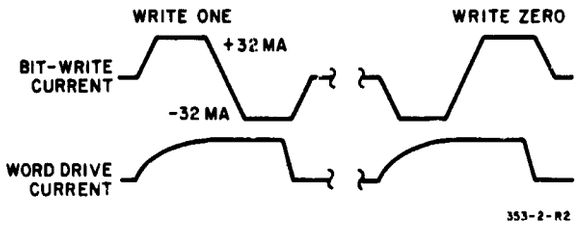

Figure 4. Phase-Modulated Write

This method of writing, called phase-modulated writing, depends upon the reversibility of the adjacent-bit interference. It eliminates this interference by always writing an equal number of 1's and 0's independent of the stored information. It also eliminates any magnetic history effect. Most magnetic storage elements exhibit a sensitivity to the polarity of the information stored in the preceding write operations. Phase-modulated writing means that every storage location experiences equal numbers of 1's and 0's in the preceding write operations.

2-2. MEMORY ORGANIZATION

The 10^8-bit memory is achieved by stacking ten 10^7-bit modules into one unit. Figure 5 shows the arrangement and organization of such a memory. Each module has its own set of driving circuits and sense amplifiers. This arrangement leads to a fast random-access memory, readily realizable mechanically, and is justified from the viewpoint of modularity and cost because the electronic circuits are still shared by a large number of bits. All modules share one set of auxiliary circuits, which include the address decoders, timing circuits, information registers, and power supplies.

The organization of the 10^7-bit memory module is shown in Figure 6. The memory plane contains 2048 word lines and 4608 plated wires. The word lines are spaced at 0.045-inch centers, while the bit lines are spaced at 0.015-inch centers. This results in a storage density of approximately 1500 bits per square inch.

The nondestructive readout property makes rewrite circuitry for each stored bit unnecessary. A word line may be made many machine words in length,

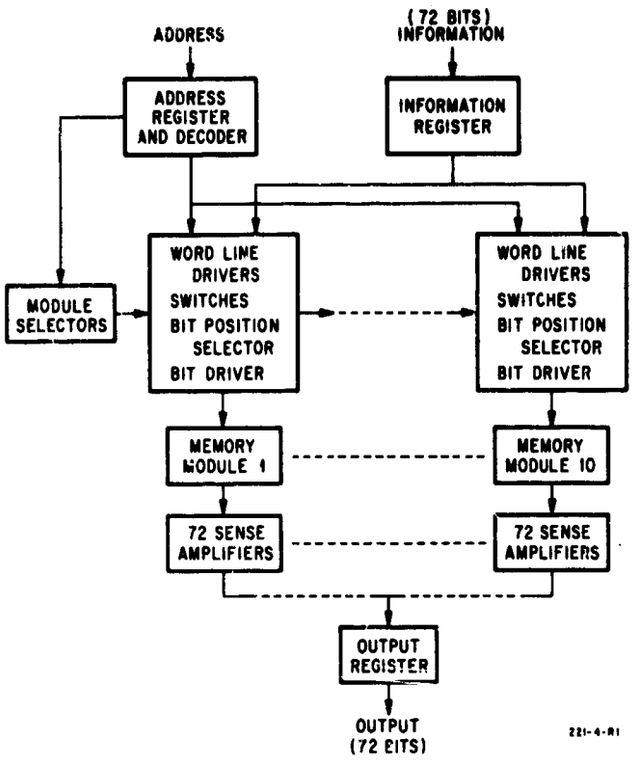

Figure 5. Arrangement and Organization of 10^8-Bit Memory

and each time all the bits in such a word-group line are interrogated, only the bits belonging to the selected word are routed by a set of gates to the sense amplifiers. After interrogation, all the originally stored information at each bit location along the word line is left unchanged. Correspondingly, the same set of gates is employed to route the bit drivers to the proper bit lines of the memory. This particular feature is illustrated in Figure 7. This property is very important because it allows a memory configuration to be chosen which leads to a minimal number of bit and word drivers and sense amplifiers.

As illustrated in a simplified version in Figure 8, the word-line selection is done by means of a transformer-diode matrix and a set of transistor switches called the A- and B-switches. The word-line matrix contains 2048 transformers whose primaries are driven by 32 A-selector and 64 B-

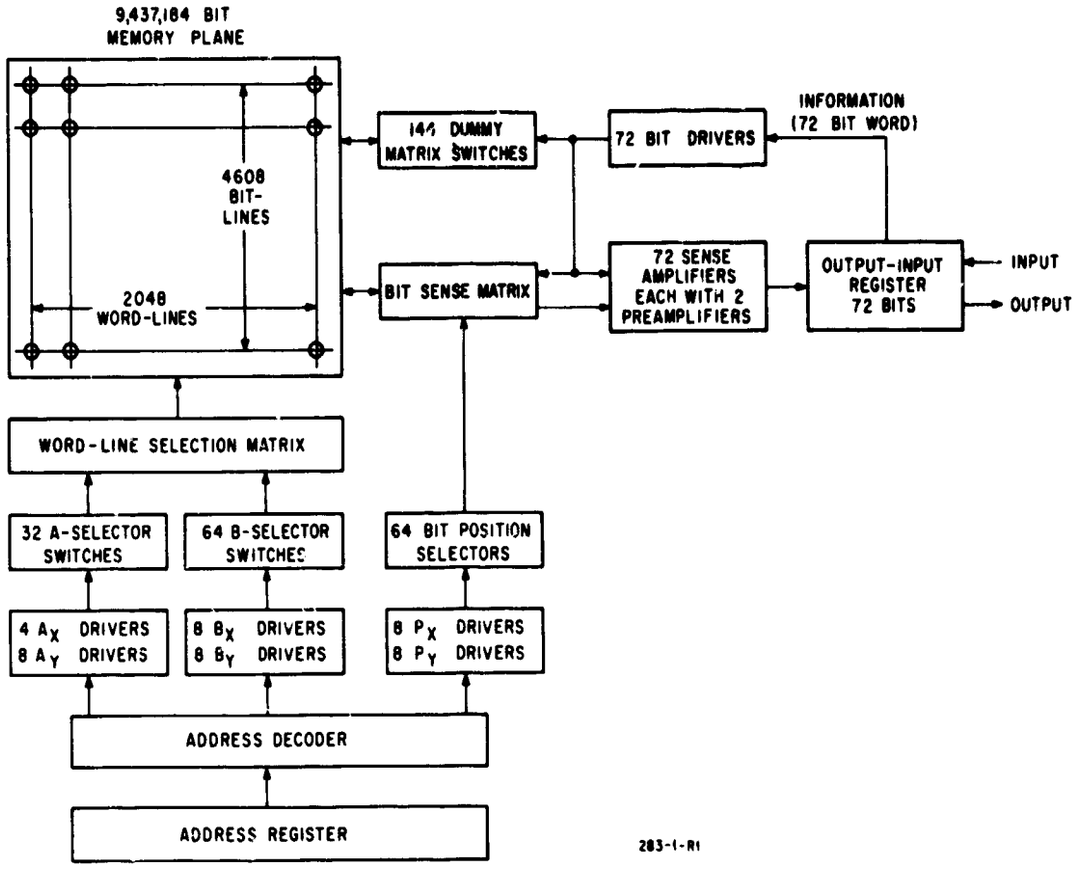

Figure 6. Organization of 10^7-Bit Memory Module

selector switches by way of a diode matrix. The bit-sense matrix consists of 4608 circuits, each containing two transistors.

The word-line matrix, bit-selection matrix, and selector switches are included physically in the memory stack; as a result, the number of connections between the memory-access circuitry and the module is reduced to a minimum.

2-3. CONSTRUCTION AND PACKAGING OF MEMORY

A sketch of the projected 10^8-bit memory is shown in Figure 9. The memory stack will consist of 10 modules, with a bit capacity of 10^7 bits per module. Each of the 10 modules will consist of a hinged memory plane, approximately 4 feet by 5 feet in the closed position. The bit-sense matrix, sense amplifier, word-line diode, and A-switch and B-switch circuitry will be incorporated as an integral part of the individual modules. The framework

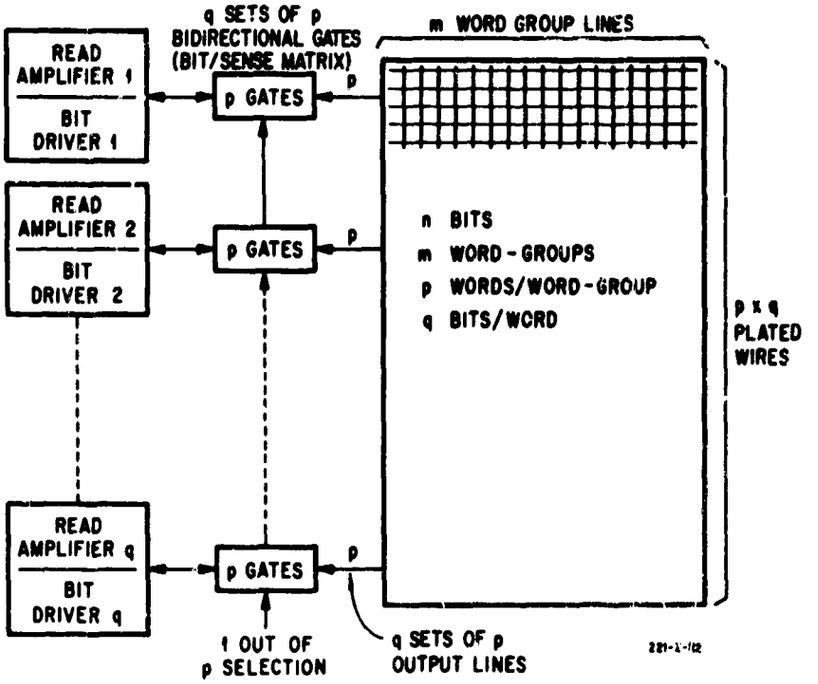

Figure 7. Modified Word-Select Memory Organization

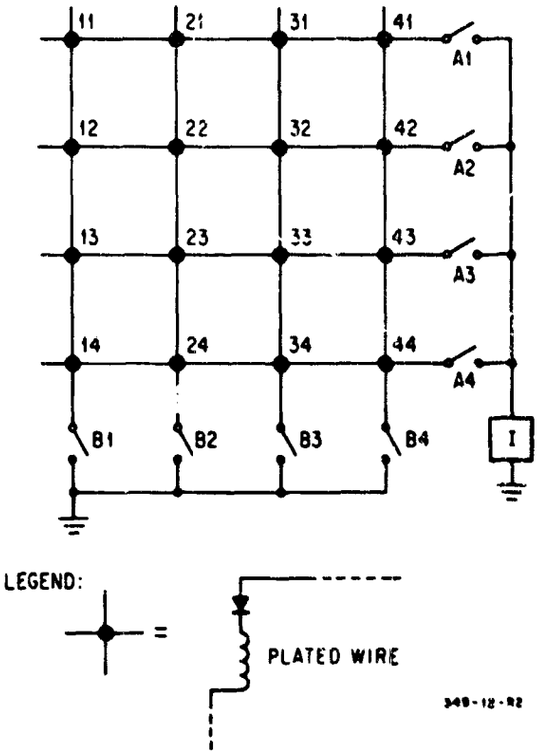

Figure 8. Word-Line Selection Matrix

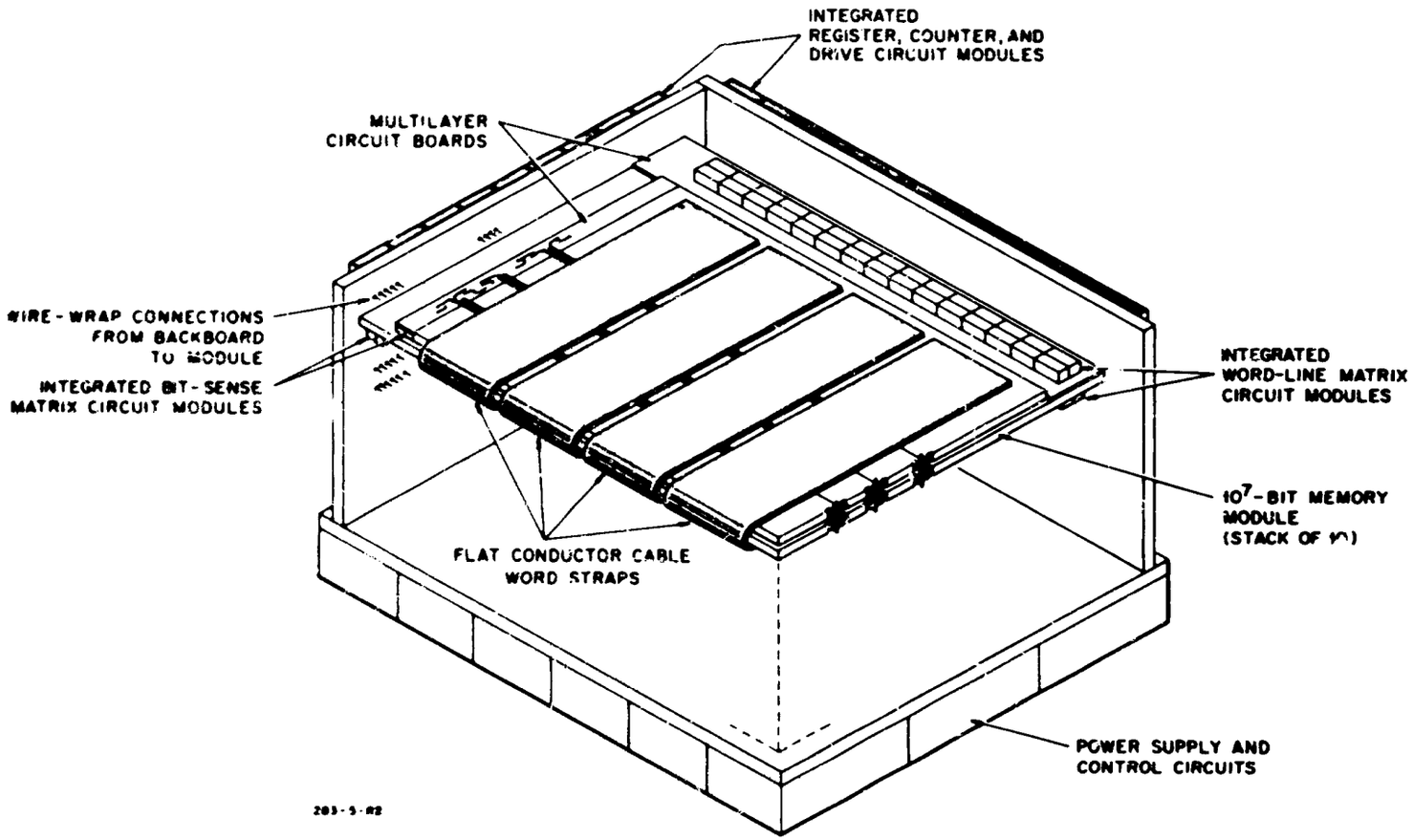

Figure 9. General Layout of the Proposed 10^8-Bit Memory

which supports the memory planes will also serve as a base for mounting those circuit modules, such as the power supply, common to all the memory modules.

The packaging may be divided into the following categories:

Memory Plane Module.

Interconnections.

Casework.

2-3.1. MEMORY PLANE MODULES

Each memory module consists of the equivalent surface of a planar memory plane with approximately a 7-foot-by-9½-foot surface. (See Figure 10.) One actual module is approximately 4 feet by 5 feet, and consists of two double-sided planes hinged along one edge. Each module consists of the following items:

Base substrate.

Plated-wire carriers and plated wires.

Word line straps.

Bit-sense matrix, sense amplifier, A- and B-switch circuitry, and word-line diodes.

The base substrate for the planes is 0.25-inch-thick aluminum honeycomb with 0.005-inch-aluminum facings. This structure provides high ratios of strength-to-weight and rigidity-to-weight.

The prefabricated Kapton-type-HF* plated-wire carriers are bonded directly on the honeycomb substrates. These carriers provide 4,896 8-foot-long tunnels capable of accepting and positioning the plated wires on 0.015-inch centers and are capable of operating at 100°C. The 8-foot dimension is the sum of the tunnel length on the front and rear surfaces of the base substrate. Plated wires on these two surfaces are interconnected along one edge of the honeycomb substrate. The plated wires are grounded at one end and connected to the bit-sense-matrix circuitry at the other end.

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*Trademark of the du Pont Company.

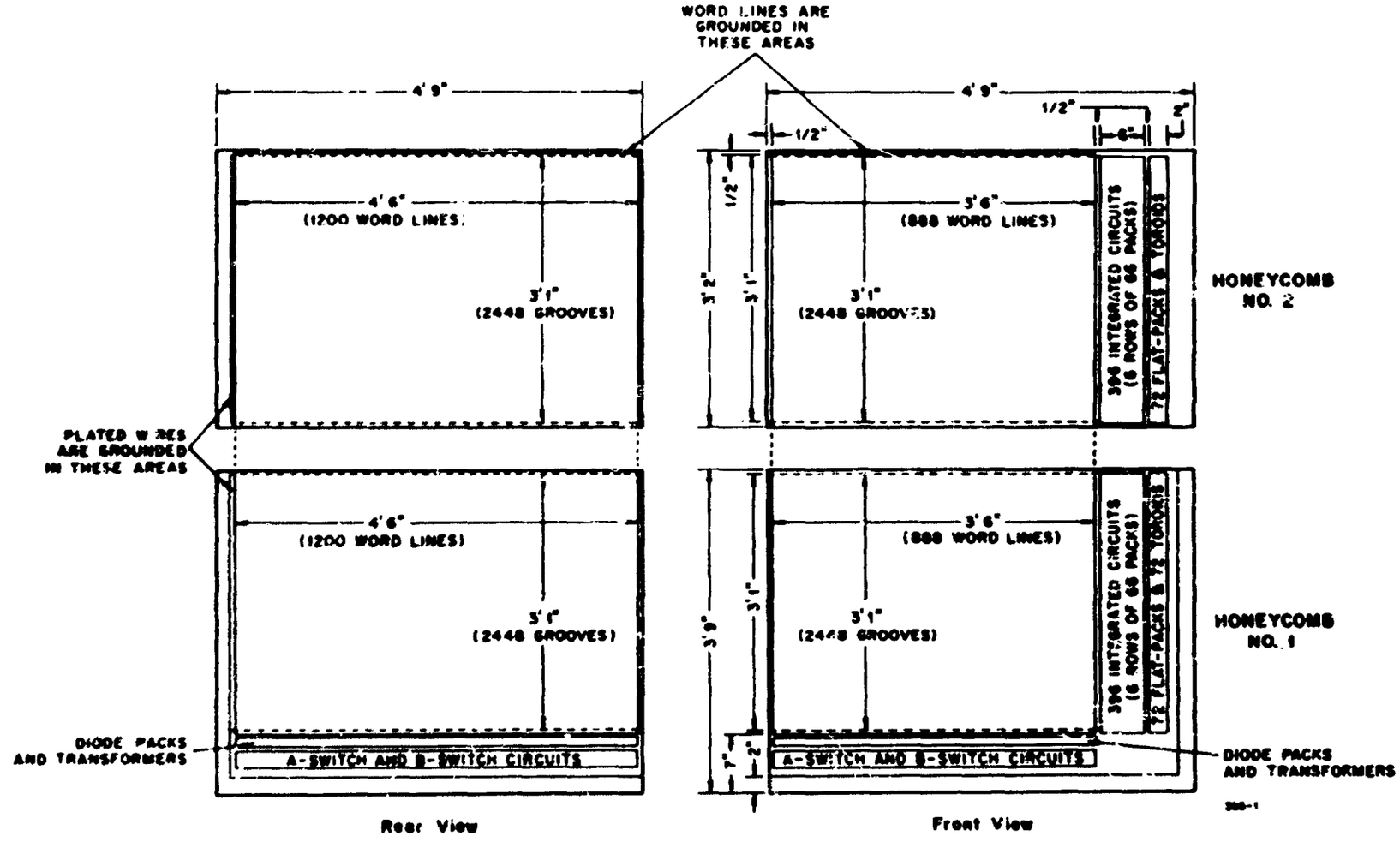


Figure 10. 10^7-Bit Module Layout

The word-line straps are formed from a prefabricated flat conductor cable. The word straps, each 8 to 12 inches wide, contain 2088 parallel copper conductors. Each conductor, 0.033 inches wide on 0.045-inch centers, is approximately 6 feet long and is bonded to one side of a 0.022-inch-thick insulating plastic film. The other side of the film is covered with a solid mu-metal shield, 0.001 inch thick. These word straps are copper conductors bonded to the plated-wire carrier so that the word line conductors are orthogonal to the plated wires. Each word line is grounded at one end and connected to the secondary of a transformer at the other end. The return path for the word lines is through the ground plane.

The bit-sense-matrix circuitry is contained in 792 flat packs mounted on the front surface of the base substrate along one end of the plated wires. The sense-amplifier circuitry consists of 144 flat packs and 144 toroids mounted alongside the bit-sense-matrix circuitry. The A- and B-switch circuits consist of flat packs mounted on the front and rear surfaces of the base substrate along one end of the word lines.

2-3.2. INTERCONNECTIONS

Interconnection of the integrated-circuit flat packs is accomplished by the use of multilayered printed wiring. Multilayer boards have been used in various Univac projects and are reasonably priced. The flat packs are connected in place directly to the surface of the multilayered board, by resistance soldering techniques.

Connections between plated wires at the edge of the honeycomb are made by mass soldering techniques. Plated wires are soldered to the multilayer boards to connect to the bit-sense-matrix circuitry.

2-3.3. CASEWORK

The framework which holds the 10^8-bit memory is made of reinforced aluminum-alloy plate. An aluminum skin, which is easily removable to allow access to the modules, is fastened to the aluminum framework. Each 10^7-bit module, although firmly held in the framework, is easily removable.

SECTION III

MEMORY PLANE CONFIGURATION

3-1. WORD LINE CONFIGURATION

The word line configuration chosen is a half-turn copper line with a mu-metal keeper on the opposite side of the line insulation. The word lines are 0.033 ±0.002 inch wide on 0.045 ±0.003 inch centers. The half-turn line is chosen over the one-turn configuration to eliminate the registration of the top half and bottom half, required by the one-turn line. Ease of mechanical fabrication is also the reason for choosing the copper lines with mu-metal backing, rather than using copper lines completely plated with mu-metal.

The characteristics of the word line, measured by sinusoidal and time domain reflectometry (TDR) techniques, are shown in Table I. Two values of characteristic impedance (Z_0) are shown for the TDR measurement, representing the initial and final values of a rising impedance characteristic.

Appendix A describes the experiments that were preliminary to determining the word line configuration and the bit line spacing.

3-2. PLATED-WIRE SPACING

The plated wires (bit lines) are 0.005 inch in diameter and are located on 0.015 inch centers. Each bit line consists of two plated wires mounted on the two sides of the memory plane and connected with a transition strip around the edge of the plane. One end of the bit line is grounded and the other end is connected to the sense amplifier and bit driver via the bit-sense matrix. Two copper cancellation wires are used with every bit group of 64 plated wires. This arrangement is described in more detail under heading 3-3. The bit line characteristics are given in Table II.

Table I. Measured Word Line Parameters

Parameter	Method of Measurement	Word Line Characteristics
Physical Length	---	6.0 feet
Electrical Delay	TDR	9.7 nanoseconds
Resistance	D-C Bridge	1.4 ohms
Inductance	General Radio Bridge, 2 megacycles	1.2 microhenries
Capacitance	Wayne-Kerr Bridge, 1 megacycle	370 picofarads
Characteristic Impedance	$\sqrt{\frac{L}{C}}$	57 ohms
Characteristic Impedance	TDR	35, 70 ohms

Table II. Measured Bit Line Parameters

Parameter	Method of Measurement	Bit Line Characteristics
Physical Length	---	8.0 feet
Electrical Delay	TDR	10.8 nanoseconds
Resistance	D-C Bridge	13.5 ohms
Inductance	General Radio Bridge, 2 megacycles	1.75 microhenries
Capacitance	Wayne-Kerr Bridge, 1 megacycle	460 picofarads
Characteristic Impedance	$\sqrt{\frac{L}{C}}$	62 ohms
Characteristic Impedance	TDR	75, 140 ohms

3-3. BIT-LINE ARRANGEMENT

In selecting the bit lines there are 2 dummy wires associated with every 64 plated wires. The dummy wires are used for noise cancellation. They are nonmagnetic wires and do not switch. The use of a plated dummy wire is required for allowing a uniform magnetic field to be developed by the word line. If the dummy wire is not magnetically plated, the adjacent regular plated wire will experience more field than those regular plated wires spaced more distantly from the dummy wire. The bit line selection scheme for a bit group is shown in Figure 11.

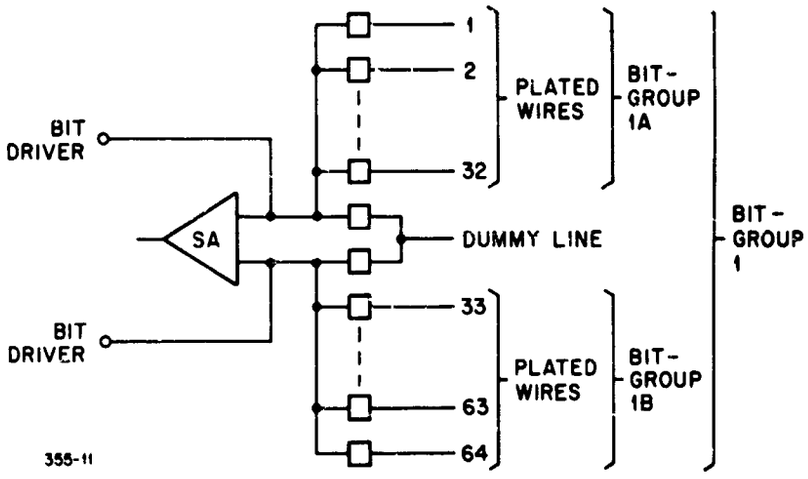


Figure 11. Plated-Wire Selection Scheme

When information is written into the memory, bit current is driven down the selected wire and down a dummy wire in order to minimize the effect of a large bit-transient voltage in the differential sense amplifier, which would occur if current flowed only in the plated wire. When information is read from the memory, identical noise is coupled into the dummy and plated wires by the word current and hence can be rejected by the differential sense amplifier.

The dummy wire associated with bit-group 1A is selected when bit lines in group 1B are being interrogated, and vice-versa. Such a symmetrical situation reduces the noise in the sense amplifier due to capacitance coupling of word-line noise through the unselected P-switches. To explain further, if all the regular plated wire were assigned to one differential input of the sense amplifier, and only the dummy plated wire to the other differential input, noise coupled to the sense amplifier through the off-impedance

of the bit-sense matrix switches would cause a noise imbalance. The symmetrical assignment of plated wires and dummy wires allows these off-impedance coupled noises to be in balance and to be rejected by the differential amplifier.

The bit driver is arranged so that the bit current in half of the bit group is of opposite polarity to the current in the other half. Therefore, within the memory plane, a 1 or 0 stored in bit-group 1A is of the opposite polarity of a 1 or 0 stored in bit-group 1B. Since the output signals from bit-group 1A are not inverted by the differential sense amplifier, while those of bit-group 1B are inverted, the output of the sense amplifier is the same for the same information stored in both bit groups. This arrangement eliminates additional logic circuitry outside the sense amplifier.

SECTION IV

MEMORY MODEL

The memory model consists of a mechanically complete 10^7-bit stack, which is the basic module required to build the 10^8-bit memory. Figure 12 shows the model and its exerciser. The lower left-hand corner of the model contains half of the diode-transformer matrix for word line selection. Above that is the flatpack bit-sense matrix for bit line selection. The memory model contains 4896 bit line tunnel structures and 2088 word lines providing 10^7 possible bit locations. Of these, 32,768 four-bit words are addressable

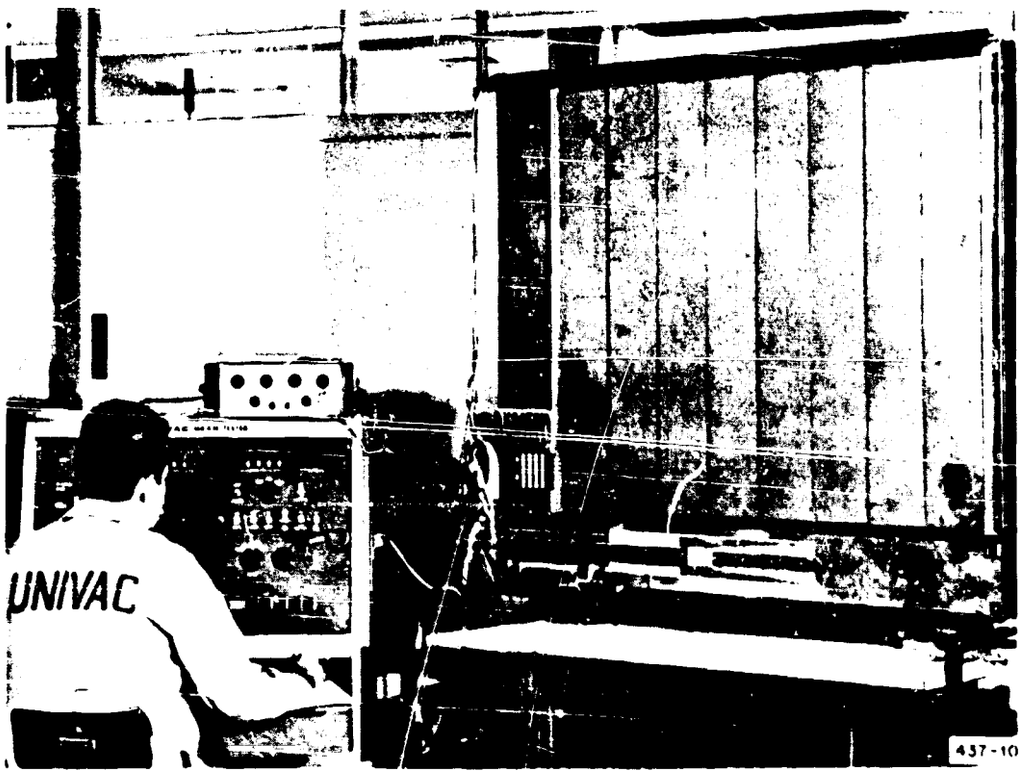


Figure 12. Memory Model and Exerciser

at the intersection of 512 word lines and 256 magnetic plated wires located at the four corners of the memory stack. (See Figure 13.) These intersections are the "four corner" locations of the bit-line and word-line.

The memory stack consists of two hinged planes with addressable bits in each of the four sides. The remaining tunnel structures contain nonaddressable plated wires in the area directly beneath the addressable word lines. This is done to obtain a worst-case loading condition on all selected word lines.

Each addressable word line contains 64 four-bit words. The word line is a 6-foot-long, 0.033-inch-wide, copper conductor on 0.045-inch centers. The bit line consists of two 4-foot plated wires in series. A flexible conductor transition piece allows the interconnections between two sides of a plane. The plated wire is 0.005 inch in diameter, on 0.015-inch centers.

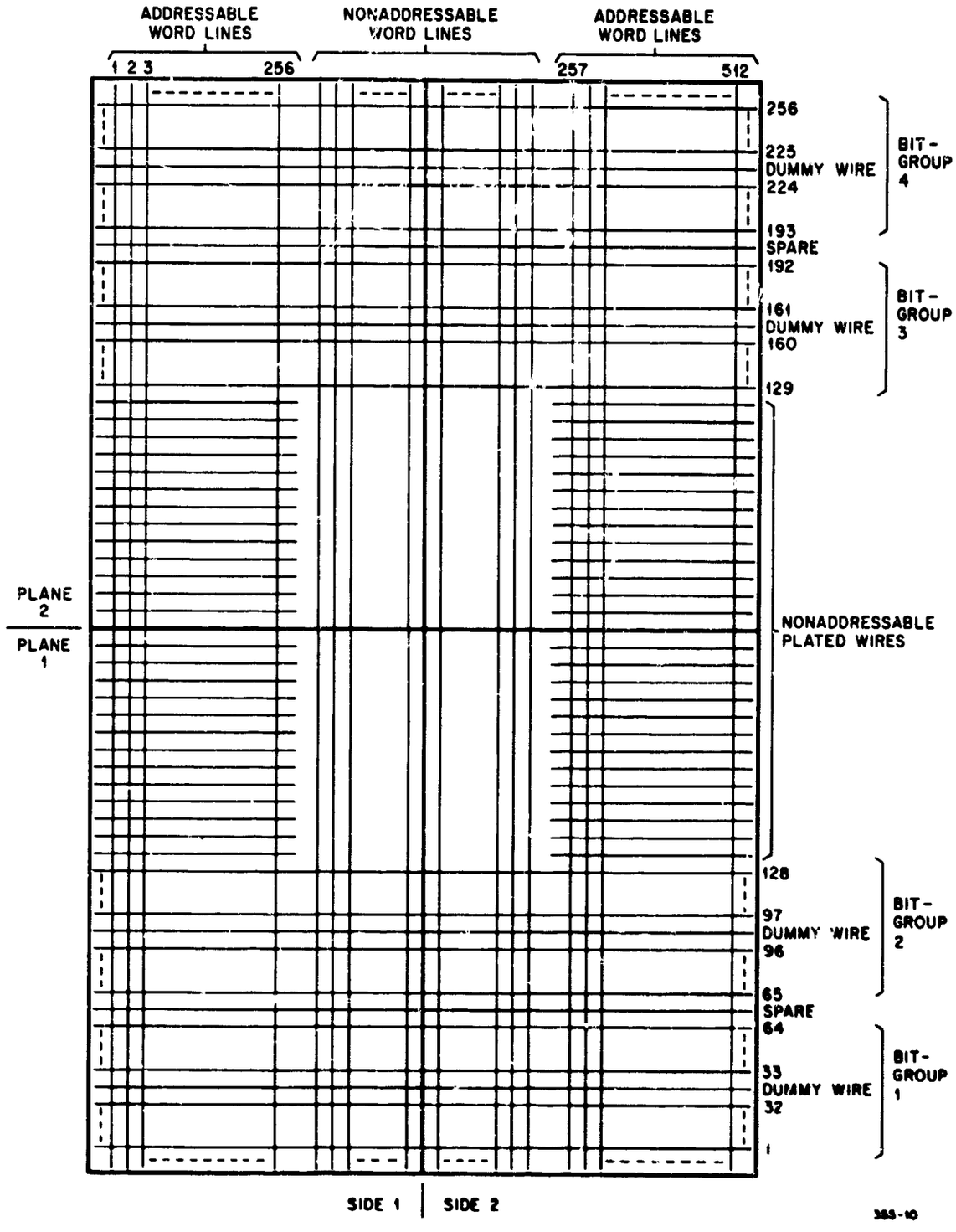


Figure 13. Diagram of Memory Model

SECTION V

ELECTRONIC CIRCUITS

5-1. INTRODUCTION

The electronic circuits described in this section are those designed for the memory model. The majority of these circuits can be employed in the full memory. Care was taken in the design of the electronic system to ensure that worst-case noise situations are encountered when the model is exercised. For example, each B-switch services 32 word lines. The noise generated by selecting a B-switch in the model would be identical to the noise in a full memory. The same concept was employed in the choice of a bit-sense matrix that matrixes 64 plated-wires into one sense amplifier and one bit driver. By adding logically parallel circuits, the memory can then be expanded to 10^7-bit module.

The electronic circuits can be divided into the following three categories:

1. Word-Current Circuits. These circuits are used to select 1 of 512 word lines and to pulse a regulated word current of 1 ampere with a maximum fall time of 50 nanoseconds.

2. Bit-Path Circuits. These circuits control the data in and out of the memory as well as performing bit selection. They include the bit drivers, sense amplifiers, and bit-sense matrix.

3. Logic Circuits. These consist of timing and control circuits.

5-2. WORD-CURRENT CIRCUITS

5-2.1. SYSTEM DESCRIPTION

Two-dimensional matrixing is used as a means of reducing the number of circuits required for selecting the word lines. A block diagram of the system is shown in Figure 14. One out of 512 word lines is selected by

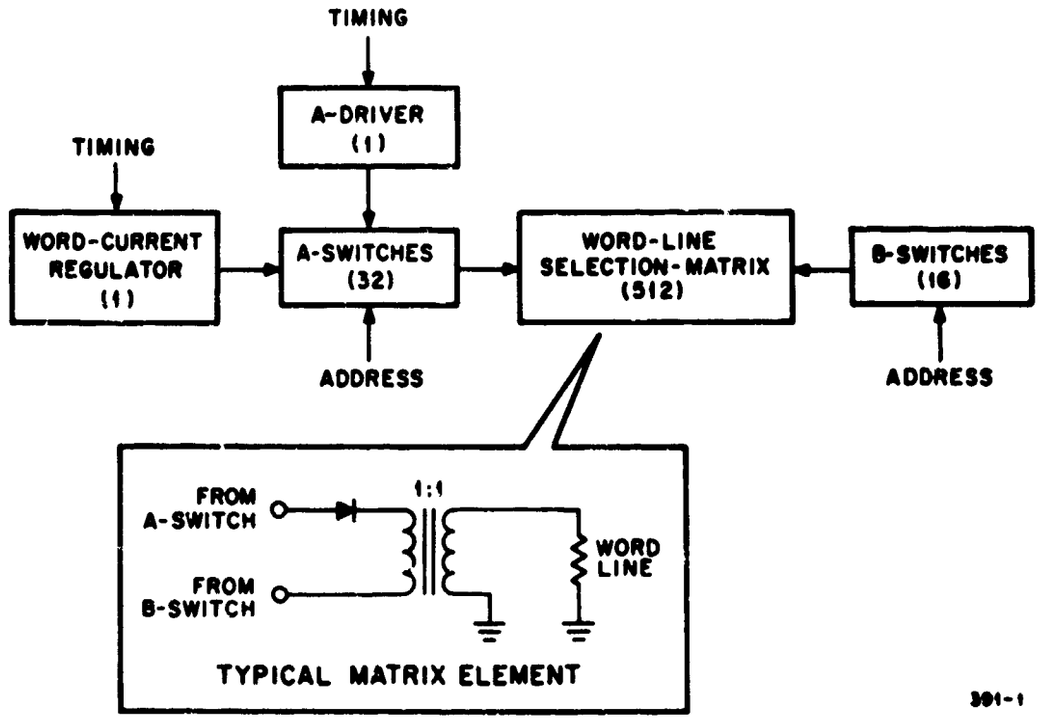


Figure 14. Word-Current Circuits, Block Diagram

addressing 1 of 32 A-switches and 1 of 16 B-switches connected to a diode-transformer selection matrix. The transformer is used to isolate the stack capacity from the B-switch. It is a simple, 1:1, No. 1041 T-060 toroid transformer, consisting of 17 turns on Ferroxcube 3E2A material. To further reduce the number of circuits, the addressing to the A-switches and B-switches is also done by means of two-dimensional selection.

The A-switch is turned on in two stages. First, the desired switch is selected by the appropriate logic levels on its address lines. Then, a current pulse from the A-driver flows through the selected A-switch and "primes" this switch to pass the output of the word-current regulator, which is turned on shortly thereafter. The current from the A-driver flows through the word-line selection matrix and forms a significant portion of the word current. The current from the A-driver must, therefore, be of well-regulated amplitude and also be of limited duration so as not to saturate the word-line transformer. The A-driver fulfills both these requirements by being a pulsed current regulator. Since the current which turns on the B-switch does not flow through the word-line transformer, it need not be well regulated.

It is possible to design a word-current system without a separate word-current regulator. In such a system, if the A-switch is turned on, full word current will flow. However, each A-switch must be capable of very good regulation of the full word current as well as very fast fall times. This would result in an A-switch being much more complex than the present one. Use of a single word-current regulator to serve a large number of A-switches provides a simpler and more economical system.

5-2.2. WORD-CURRENT REGULATOR

5-2.2.1. CIRCUIT CRITERIA: The word-current regulator must supply well-regulated pulses of current to the primary winding of a 1:1 transformer whose secondary winding is connected to a word line. The amplitude of this current is about 1000 milliamperes, and the equivalent inductance of the word line and the associated wiring is on the order of 2 microhenries. For maximum signal amplitude on readout, it is important that the word-current pulse have a fast switching time and a sharp top corner. Attempts to achieve this on the leading edge of the pulse cause ringing and, hence, an overshoot of the desired amplitude. If uncontrolled, this overshoot could lead to destructive readout. Furthermore, the supply voltage from which the circuit operates must be at least $L \frac{di}{dt}$, where L is the word-line inductance. Substituting 2 microhenries and 50 nanoseconds into this expression yields 40 volts. The regulating transistor would have to withstand this voltage plus that generated during the fall time of the current. For these reasons, it was decided to use the trailing edge of the word current for reading information out of the memory.

Reading on the trailing edge provides the following advantages:

a. A sharp top corner on the word current is more easily obtained.

b. Word-current overshoot may be controlled by slowing the leading edge.

c. A lower supply voltage is needed to ease the semiconductor requirements.

5-2.2.2. CIRCUIT DESIGN: The circuit presently being used is a variation of a zener diode current regulator. This type of circuit is shown in its basic form in Figure 15. The current through R1 is designed to depend on the breakdown voltage of zener diode D1, on the base-emitter drop of Q1, and on the resistance itself. The output current is thus a function of the

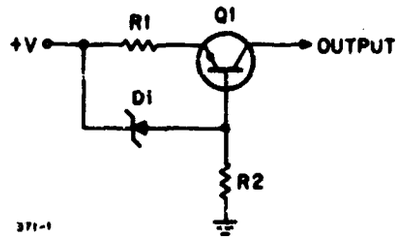


Figure 15. Basic
Current-Regulator Circuit

aforementioned quantities and of the alpha of transistor Q1. Since all these quantities are quite stable, an output current independent of power supply and of load impedance variations can be obtained.

Adapting this basic regulator to the proposed memory results in the circuit design shown in Figure 16. Design goals in this adaptation include the following considerations:

a. No standby power.

b. Slow, controlled rise time, and very fast fall time.

c. Remote current-amplitude adjustment.

d. Accurate pulse-width control.

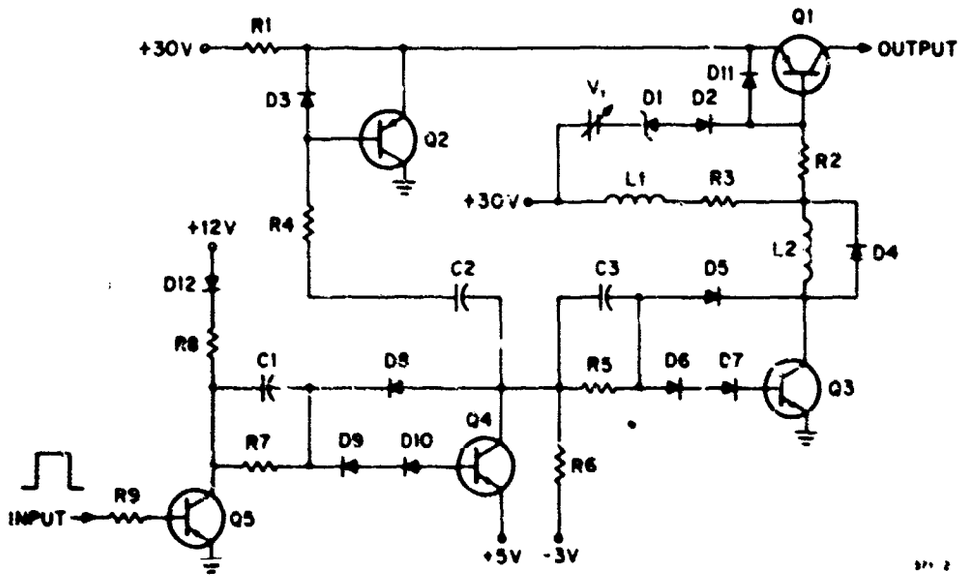
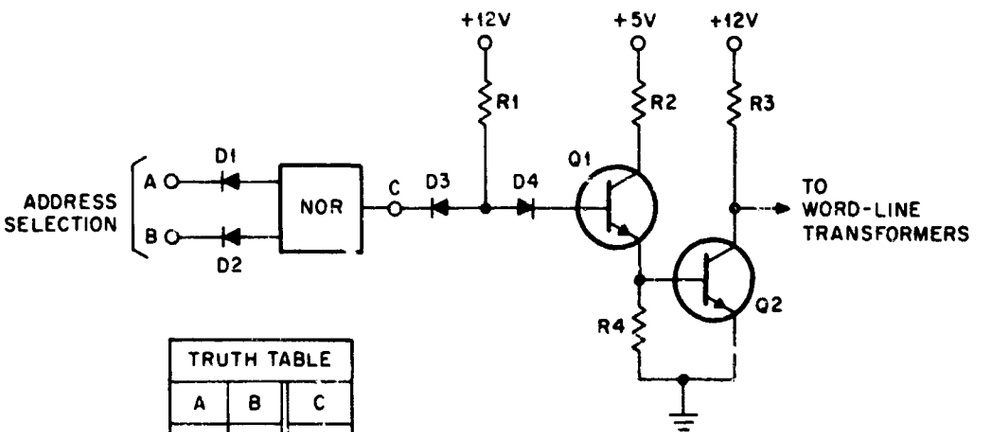


Figure 16. Word-Current-Regulator Circuit

The use of complementary stages biased off quiescently achieves the aim of no standby power. By design, transistor Q1 does not saturate; anti-saturation diodes D5 through D10 in the two other high-level stages eliminate storage time; thus, good pulse-width control is achieved. Inductor L2 slows the current rise time, and L1 stores clean-up current for Q1 to speed turn-off. Transistor Q2 is turned on momentarily at the trailing edge of the pulse and diverts the current flowing through resistor R1. This, too, speeds the fall of the word current. Voltage V_1 is a floating power supply which serves to vary the word current. The voltage adds to the zener diode voltage. This supply is remotely adjustable by means of a variable resistor in the exerciser and is used to demonstrate the operating range of the model. This variable supply will not be used in a final memory. This circuit yields a rise time of about 150 nanoseconds and a fall time of approximately 30 nanoseconds.

5-2.3. B-SWITCH

The B-switch uses a Univac-designed monolithic logic gate for selection. The output of this gate drives a modified Darlington pair in order to provide the necessary high-level output. A schematic of the circuit is shown in Figure 17. The B-switch is selected when both address inputs are low (ground); in this case, transistors Q1 and Q2 are enabled. From system noise considerations, it is desirable to drive the collector of Q2 as close to ground as



TRUTH TABLE

A	B	C
H	H	L
H	L	L
L	H	L
L	L	H

Figure 17. B-Switch, Schematic Diagram

possible. It is for this reason that a direct Darlington connection of Q1 and Q2 was not used. Such a configuration would have raised the output voltage to V_{BE2} plus V_{CE1}. The NOR gate is available as four gates in a flat pack.

When a B-switch is unselected, its output is referenced to +12 volts. This back-biases the unslected matrix diodes.

5-2.4. A-DRIVER

The A-driver, shown schematically in Figure 18, is a current regulator very similar to the basic circuit described under heading 5-2.2. Its output current is limited to $I_{MAX} = (V_{D5} - V_{D4} - V_{BE2})/R_4 \approx 100$ milliamperes. The term "limited to" is used here since the driver will deliver less cur-

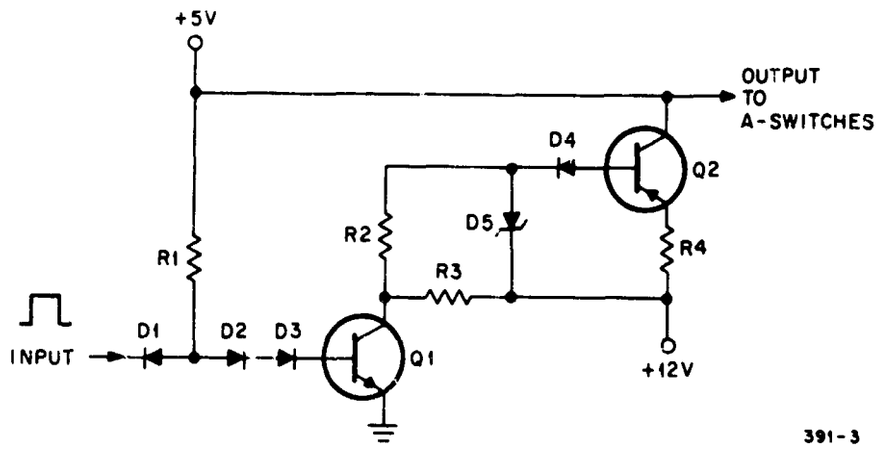


Figure 18. A-Driver, Schematic Diagram

rent than this, should the voltage across the load be higher than $12 - I_{MAX}R_4$. In other words, a current regulator will deliver no more than its maximum design current but will deliver less than this if less is demanded by the load. This will be discussed further under heading 5-2.5. Diode D4 was added to improve the transient behavior of the driver.

5-2.5. A-SWITCH

A schematic of the A-switch is given in Figure 19. The switch is selected when both address inputs are high: Q1 is turned on and thus provides a path for the base current of Q2. This base current flows when the A-driver turns on; thus, Q2 operates in the common-base mode. The current

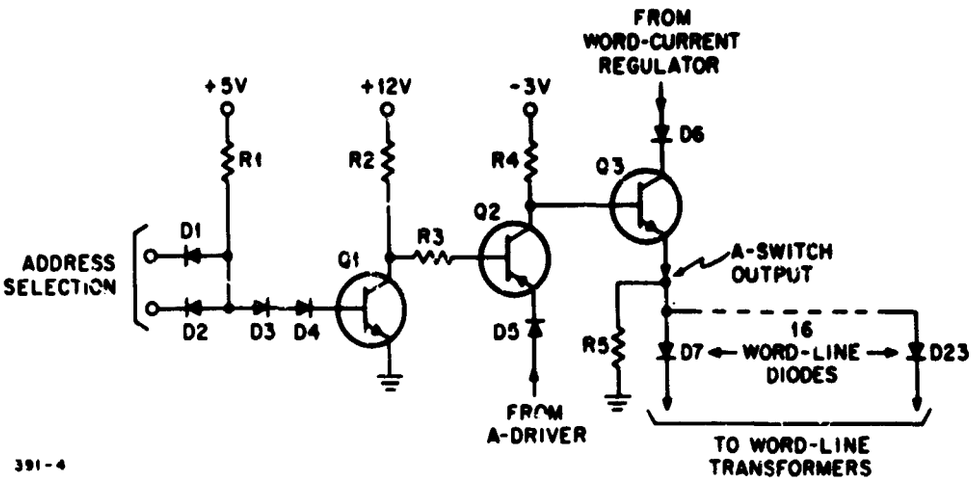


Figure 19. A-Switch, Schematic Diagram

from the A-driver flows through Q2 of the selected A-switch into the base of Q3, through one of the matrix diodes D7 through D23, into its word-line transformer, and then to ground by way of the selected B-switch. Once this current flow has reached equilibrium, the word-current regulator is pulsed. Its output current flows through Q3 of the A-switch and adds to the current from the A-driver, the two thus comprising the word current.

When the word current regulator is turned on, it attempts to build up word current at a rapid rate. Since the word line is inductive a high back emf appears at the emitter of Q3. This emf (plus several semiconductor voltage drops) is seen at the output of the A-driver and lowers the amount of current which the driver can supply, as described under heading 5-2.4. With a reduced base current, Q3 in the A-switch can no longer pass the full amplitude of the word-current regulator output. The rate of word-current rise is thus slowed; the back emf drops slightly, the A-driver current increases, and the word current rises. In this manner, the 12-volt supply used in the A-driver serves to control the rise time of the word current by limiting the back emf across the word-line transformer.

Since variations in the base current of Q2 of the A-switch reflect directly in the word current, a high-gain transistor was selected for Q2.

Resistor R5 serves to reference the anodes of the word-line diodes to ground.

5-2.6. WORD-LINE SELECTION MATRIX

A 1:1 word-line selection transformer was used since either a current or a voltage step-up would have caused semiconductor problems in the word-current circuits. Furthermore, since a bifilar winding is used to minimize leakage, a 1:1 turns ratio simplifies the fabrication of such a transformer. The number of turns was based on a calculation of transformer saturation for the pulse width and load to be encountered.

To prevent noise induced in unselected transformers connected to a selected B-switch from coupling to the plated wires, the phasing of the transformer secondaries are alternated on alternate word lines. In this manner, any coupled noise from one unselected word line will be approximately balanced by an equal and opposite noise on the adjacent line.

5-3. BIT-PATH CIRCUITS

5-3.1. BIT-SENSE MATRIX

5-3.1.1. USE OF HYBRID INTEGRATED CIRCUIT. The bit-sense matrix is the circuit which permits one bit driver and one sense amplifier to serve many plated wires. One circuit is required for each wire. Since the wires are located on 0.015-inch centers and since the bit-sense matrix must pass the low-level sense signals, it is highly desirable to make the matrix circuits as physically compact as possible. Indeed, for the number of wires proposed in the total memory, it becomes imperative to depart from discrete component circuitry to avoid inordinately long wiring paths.

To achieve compactness, a hybrid integrated circuit has been designed and fabricated by the Physics and Materials Section at the Univac Engineering Center, Blue Bell, Pennsylvania. It contains thin-film resistors, conductors, and chip transistors. Six circuits are contained in a 1/4-inch-by-3/8-inch flat pack having 14 leads.

5-3.1.2. CIRCUIT DESCRIPTION. A schematic drawing of the bit-sense-matrix package is shown in Figure 20. Three bidirectional switches in a package are selected by applying positive and negative potentials to the proper pair

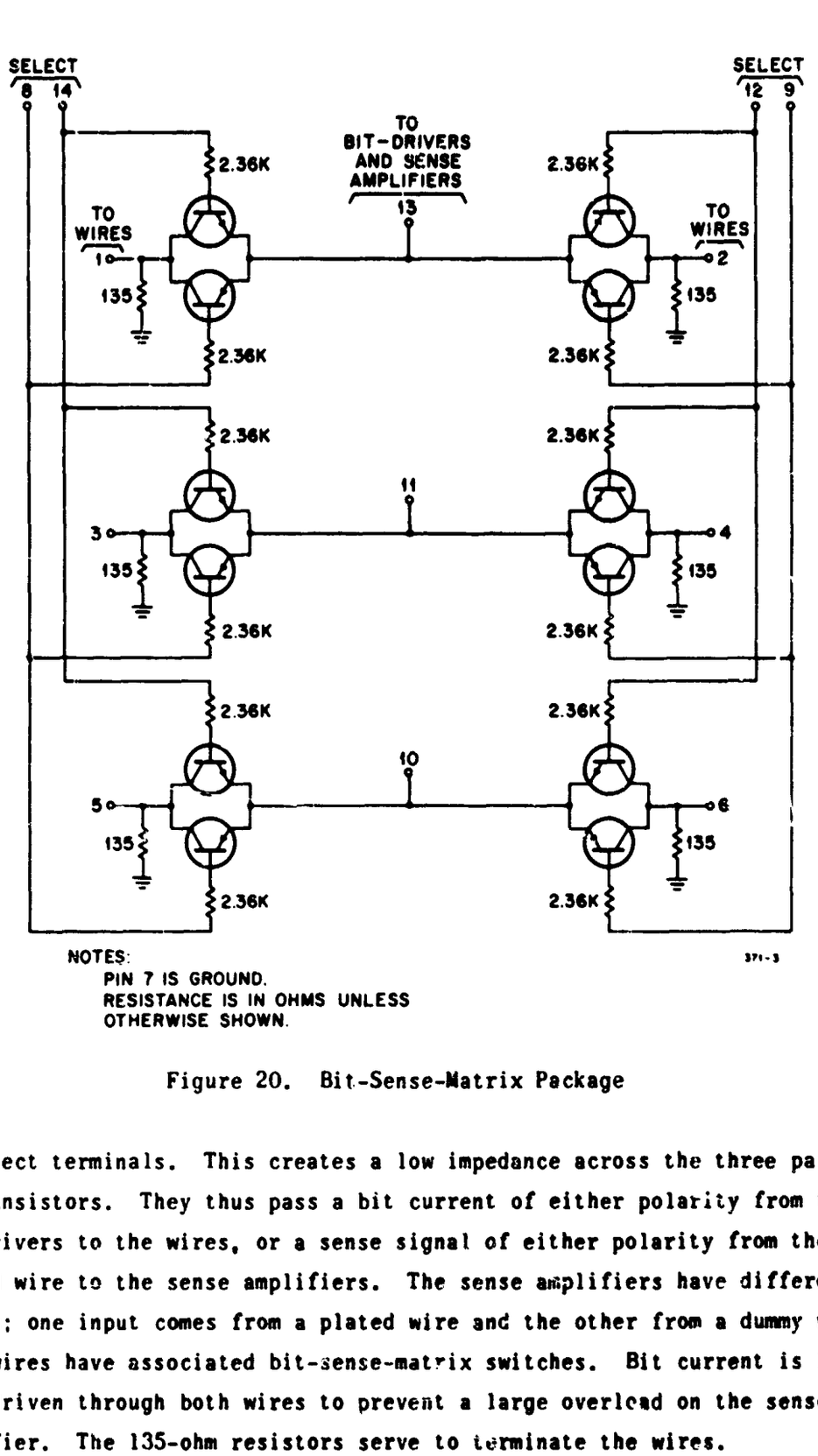


Figure 20. Bit-Sense-Matrix Package

of select terminals. This creates a low impedance across the three pairs of transistors. They thus pass a bit current of either polarity from the bit drivers to the wires, or a sense signal of either polarity from the plated wire to the sense amplifiers. The sense amplifiers have differential inputs; one input comes from a plated wire and the other from a dummy wire. Both wires have associated bit-sense-matrix switches. Bit current is likewise driven through both wires to prevent a large overload on the sense amplifier. The 135-ohm resistors serve to terminate the wires.

Desired characteristics of the transistors include low capacitance in the cutoff state, so that signals generated in unselected wires during a read instruction are not coupled to the sense amplifiers. At least one of the transistors in each pair must have a low dynamic impedance at low signal levels to avoid excessive attenuation of the sense signals. During a read instruction, base current flows from the NPN transistor to the PNP transistor, with only the difference between the two base currents flowing elsewhere. To achieve a balance, it is important that the 2.36-kilohm resistors be of close tolerance. Also during a read operation, any difference between the collector-emitter voltages (offset voltage) of the matrix switches connecting the plated wire and the dummy wire to the sense amplifier appears as a d-c signal to the amplifier. The offset voltage of the transistors must therefore be minimized. These requirements, tight complementary transistor specifications and close resistor tolerances, are beyond the present capabilities of monolithic silicon technology. Hybrid thin-film circuitry is well-suited to this application.

5-3.1.3. CIRCUIT FABRICATION. The hybrid circuits are fabricated on a glass substrate. Onto this a layer of tantalum and a layer of gold are sputtered. Through the use of precise photographic masks, the proper resistor and conductor patterns are etched. The substrate is then heated to develop a protective layer of oxide on the newly exposed tantalum resistors. By passing a current through the resistors and thus further oxidizing the tantalum, they are trimmed to their final value. The substrate is then diced into individual groups of three bidirectional switches, and the transistor chips are attached. The circuits are then mounted in flat packs, and leads are attached between the package and the circuits and between the transistor elements and their pads. The package is then sealed and tested.

5-3.2. BIT-SENSE-MATRIX DRIVER (BSMD)

The bit-sense-matrix driver selects the bit-sense matrix. The bit-sense-matrix driver is shown in Figure 21. Logical inputs are received from the memory exerciser to produce, via the BSMD, bipolar outputs required for driving the bit-sense-matrix switches. Each output drives 4 matrix switches in parallel while providing a back bias of 3 volts for the matrix switches when they are not selected. There are 64 bit-sense-matrix drivers (the same number as in a full 10^7-bit module) in the model.

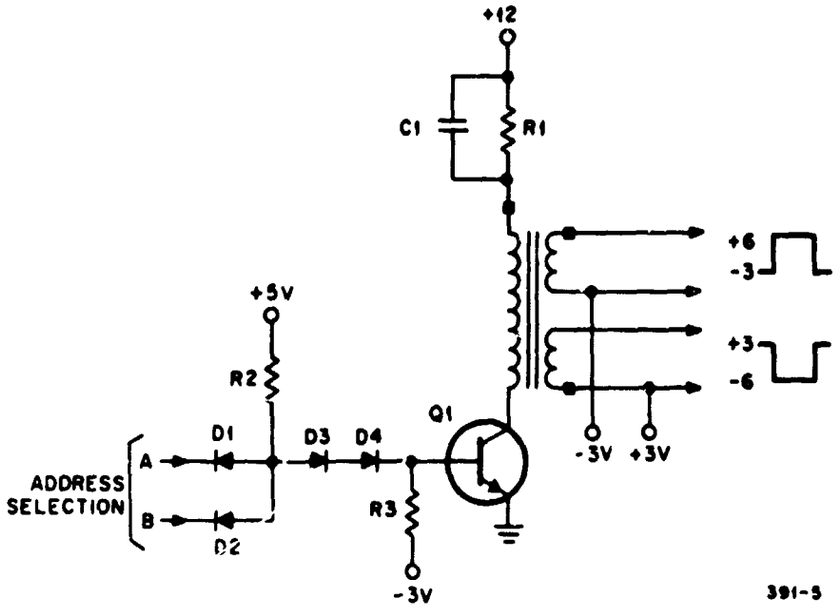


Figure 21. Bit-Sense-Matrix Driver, Schematic Diagram

Diodes D1 and D2 form an input AND gate, whereas D3 and D4 produce level shifting. Resistor R1 limits the collector current through Q1 to prevent its burnout in the event that there is a fault and Q1 is maintained in an on condition. During normal operation, capacitor C1 provides a bypass for R1 so that the full supply voltage would appear across the transformer. The turns ratio of the transformer provides a 9-volt output swing.

5-3.3. BIT DRIVER

The bit driver is shown in Figure 22. The phase-modulated-write method used in this memory system requires the writing of the complement information first, followed by the writing of true information during the writing of a bit. Therefore, if a 1 is to be written in a bit location, a 0 is written first, followed by the writing of the 1. Transistors Q1 and Q2 (see Figure 22) are pulsed sequentially on and off by the information generator in the memory exerciser during a write-1 instruction. This generates, in turn, a negative and then a positive current in the secondary windings of the transformer. The sequence of pulsing Q1 and Q2 is reversed for a write-0 instruction.

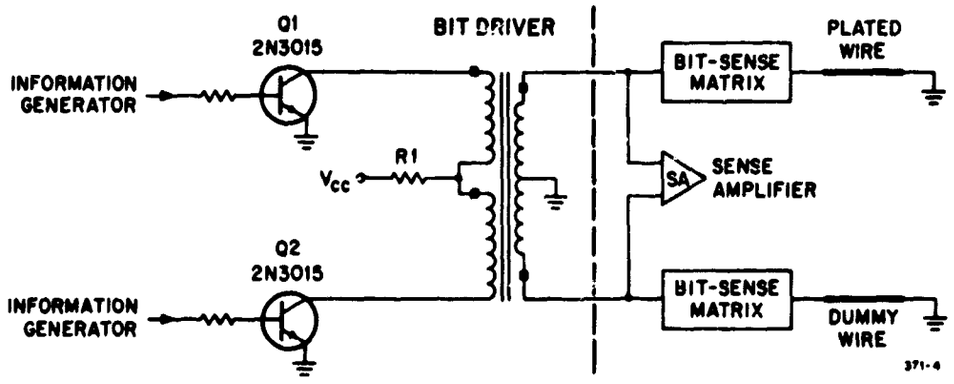


Figure 22. Bit-Driver Design

With a nominal collector-supply voltage (V_{cc}) of +12 volts, resistor R1 limits the current in the primary winding to 64 milliamperes. This allows the secondary to deliver 32 milliamperes to the plated wires and 32 milliamperes to the dummy wires. In order to provide a means of varying the bit current and thereby determining the operating margins of the memory, V_{cc} is adjustable from the front panel of the exerciser. This arrangement of the bit current prevents the injection of a large, differential, bit-transient signal in the sense amplifier, thereby minimizing the recovery time. This arrangement of the bit driver allows a cycle time of a few microseconds.

The transformer consists of two 6-turn bifilar windings located on opposite sides of the core corresponding to the primary and secondary windings. These windings are intraconnected to produce the proper phase.

5-3.4. SENSE AMPLIFIER

5-3.4.1. SYSTEM GOALS. An integrating sense amplifier is used for the memory. This detects the time integral of its input rather than its peak amplitude. Such an amplifying system has several advantages in a large memory, including the following:

a. Crosstalk from readout signals in adjacent wires is cancelled. Since all plated wires under a word line are read out simultaneously, crosstalk from wires adjacent to the one being interrogated can subtract from the peak of the desired signal. It can be shown, though, that the net area under this crosstalk is zero so that an integrating sense amplifier minimizes its effect.

b. Word line noise coupled to the plated wire has, to a first order, a zero time integral. It, too, is cancelled out in the amplifier.

c. Dependence on the fall time of the word current is minimized. Since the area of the plated-wire readout signal is a function of word current amplitude but not of speed, use of an integrating sense amplifier relaxes the requirements on the word circuitry.

d. Approximately equal output area results from readouts at all positions along the plated wire. A readout from the grounded end of the wire yields a single pulse, while transmission line behavior causes the readout from the other end of the wire to reach the sense amplifier as two like-polarity pulses of lower amplitude. If line attention is neglected, the total area of both readouts is the same, so that the integrating amplifier gives identical outputs.

e. Strobe timing is less critical with an integrating sense amplifier. A peak-detecting amplifier must have as narrow a strobe as possible to prevent its triggering on noise. With the signal delays along an 8-foot bit line, narrow strobing would be difficult. The integrator, however, holds its maximum output sufficiently long to permit a wide strobe and looser tolerances on its timing.

5-3.4.2. GENERAL DESCRIPTION. A block diagram of the sense amplifier is shown in Figure 23. The transformer input to the preamplifier is required to allow the proper d-c biasing of the preamplifier. It also provides common-mode noise rejection. The gate is a low-impedance shunt which is

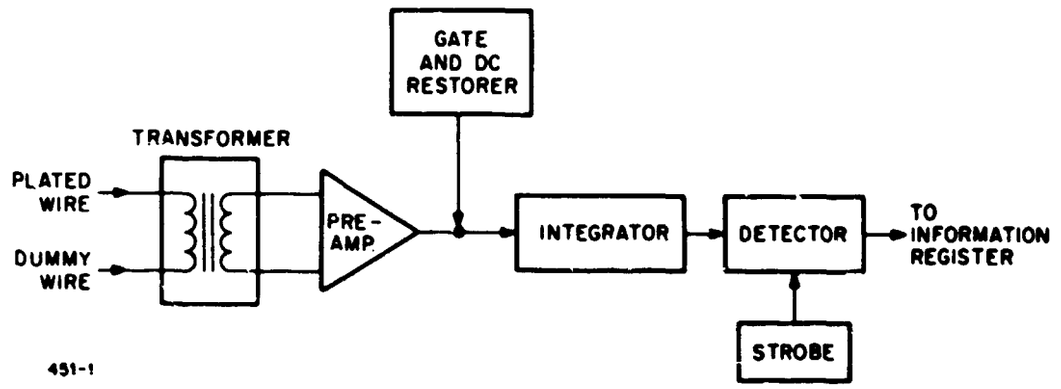


Figure 23. Block Diagram of Sense Amplifier

normally closed. This provides a d-c zero reference at the integrator output. During the interval when the wire signal is to be sensed, this gate is opened. The integrator then charges up, and the gate is closed. Next, the strobe is energized, and the detector provides an output pulse for one polarity of plated-wire signal and no pulse for the other polarity.

5-3.4.3. CIRCUIT DESCRIPTION. A complete schematic of the sense amplifier is shown in Figure 24. As can be seen, the major components are

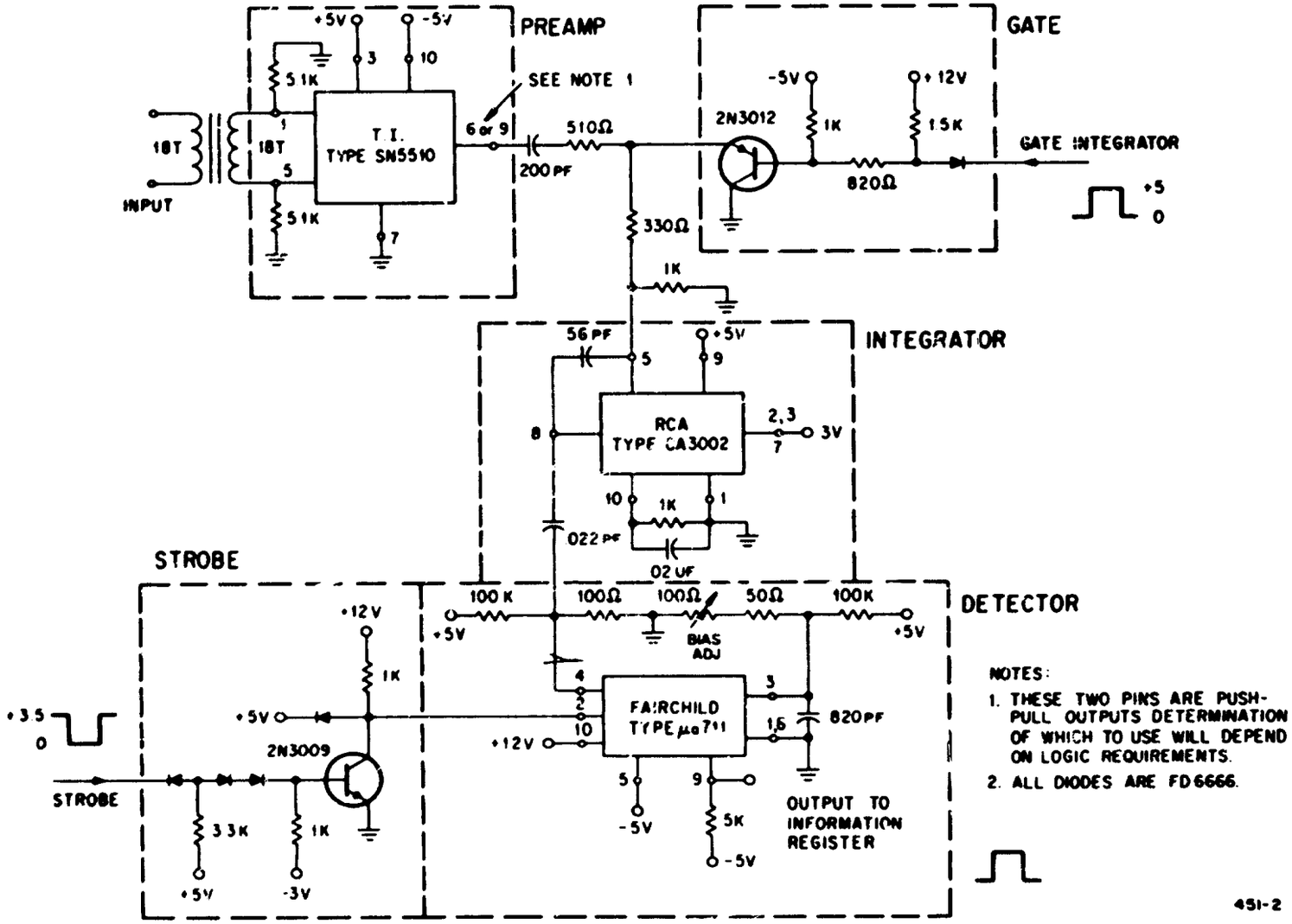


Figure 24. Sense Amplifier, Schematic Diagram

off-the-shelf integrated circuits. To achieve versatility, these circuits generally omit input biasing networks. Coupling capacitors must also be added. The transistor which serves as the gate is operated as a chopper in the inverted mode. This technique provides very low impedance to ground when the transistor is on and could not have been achieved with a standard integrated circuit. The strobe circuit, while available as an integrated circuit, was more readily built from discrete components.

A Texas Instruments SN 5510 serves as the preamplifier. It has a bandwidth of 40 megacycles, more than adequate for the purpose, and a voltage gain of about 80. Only one-half of its differential output is used. A feedback capacitor was added to the RCA CA-3002 linear amplifier to convert it to an integrator. The Fairchild μA 711 is a high-gain amplifier with strobe provisions. It has a very small linear range, about 3 millivolts at the input, and is thus useful as a pulse shaper. The bias adjustment is used to set the desired trigger level. When the signal input exceeds this level, the output follows the strobe pulse.

Tests of the sense amplifier indicate that it achieves all design goals.

5-4. LOGIC CIRCUITS

The logic circuits used in the memory and the exerciser are TTL integrated circuits, designed by Sylvania and designated SUHL-I. It was found that a saving can be realized by buying these chips already mounted on module cards. These cards, containing SUHL-I circuits, are purchased from Control Logic Company.

SECTION VI

MEMORY EXERCISER

6-1. GENERAL

A memory exerciser was designed and constructed. Figures 25 and 26 show the control panel and the back view, respectively, of the exerciser.

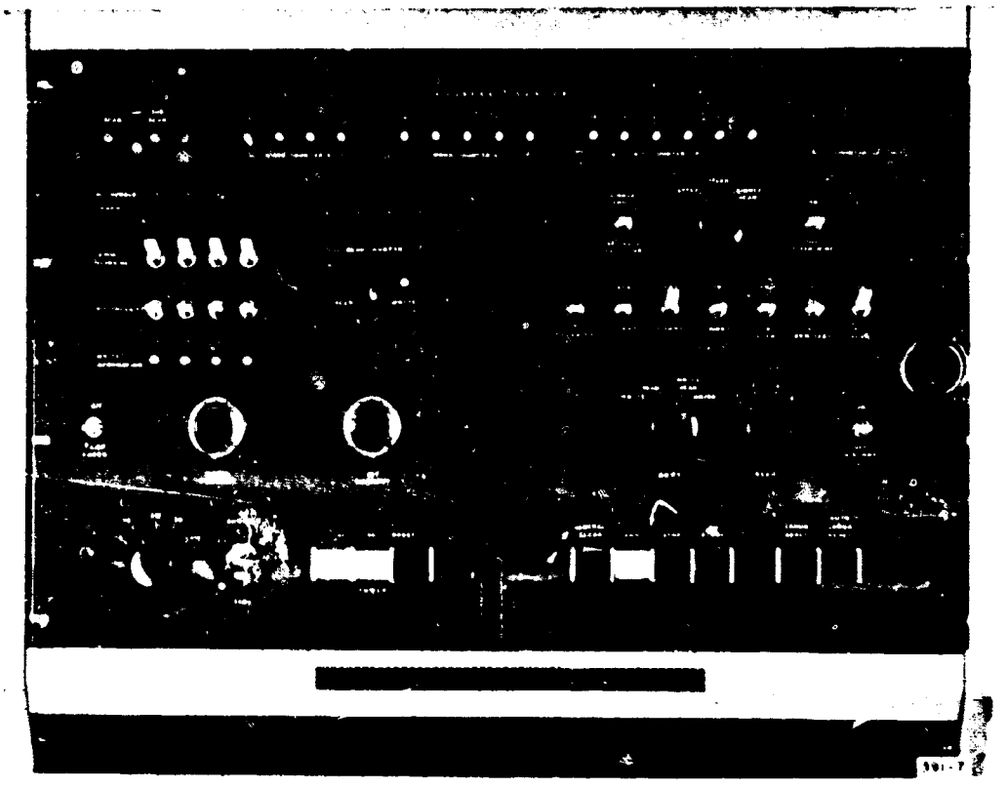


Figure 25. Memory Exerciser Control Panel

The memory exerciser is designed to simulate the effects of a random-access computer operation on the memory circuits and elements. The exerciser generates various information patterns which are sent to the memory, and then

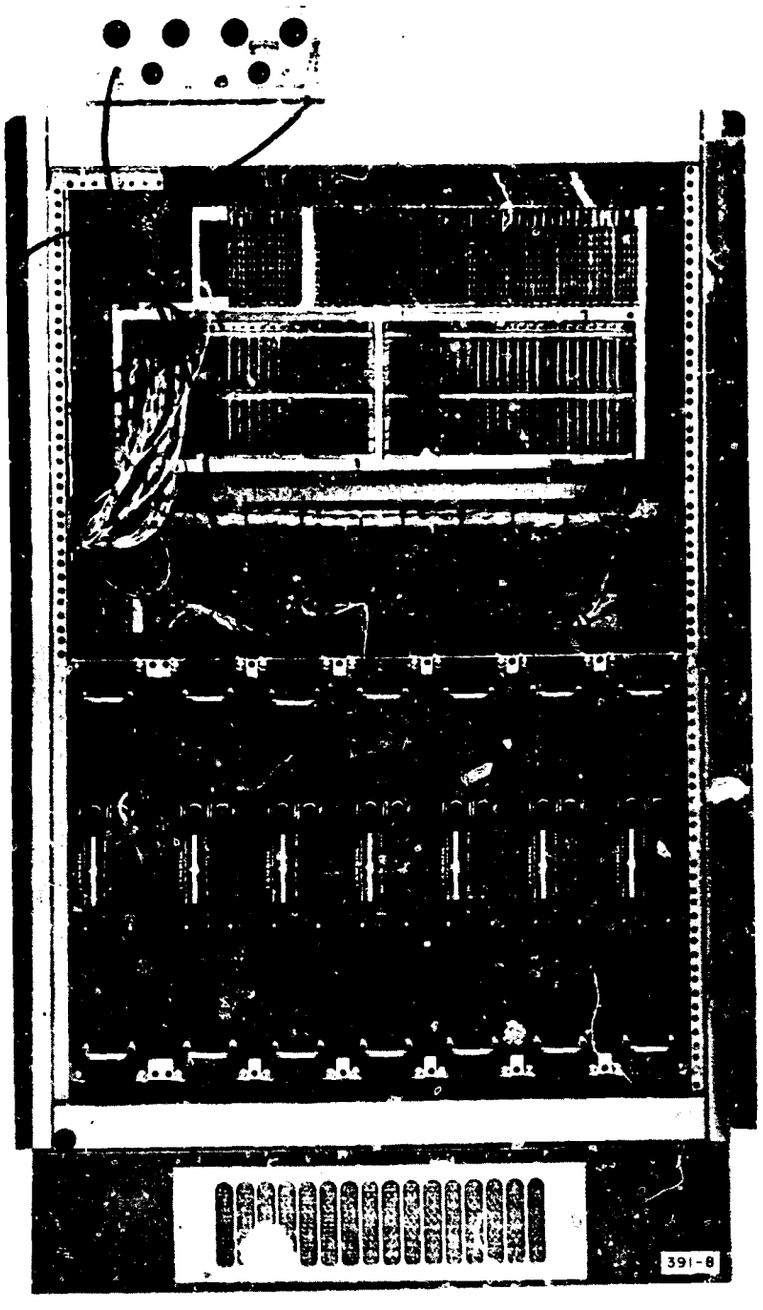


Figure 26. Memory Exerciser, Back View

checks that this information is properly written and read from the memory. If a malfunction should occur in any of the memory circuits or the plated-wire elements, the exerciser would stop. The exerciser indicator lights then would give a complete analysis of the error condition.

6-2. EXERCISER ORGANIZATION

The exerciser is designed to check 131,072 bits of information divided into 32,768 4-bit words. Information is sent to and received from the memory in a 4-bit parallel mode at a rate of 20 kilohertz or faster.

The exerciser is divided into four main logical blocks consisting of the binary address counter, information generator, bit information paths and detection circuits, and the timing and control circuits.

The binary address counter supplies the 15-bit address to the memory, determines whether information is to be written into or read from the memory, and supplies inputs to the information generator.

The information generator supplies the values of 1 or 0 at each memory address to the bit information path. It is controlled by the address counter and the front panel controls. In this way, various patterns of 1's and 0's can be written throughout the memory at various addresses.

The bit information path and detection circuits control the information between the exerciser and the memory. Information is transmitted to the memory during a write command in accordance with the output from the information generator. During a read command, the detection circuits compare the information readout to that stored at a given bit location and indicate the error, if any should occur.

The control circuits provide timing and miscellaneous control signals for the tester and memory.

6-3. OPERATION MODES

The tester is capable of supplying various information patterns and modes of operation. These modes are WRITE (W), READ (R), WRITE/READ (W/R), WRITE/READ/SUBSCAN (W/R/SS). The W and R modes simply allow information to be written into or read from the memory. The W/R mode allows the exerciser to exercise each address (four bits) by writing information into the bit position and immediately reading it out a predetermined number of times. The W/R/SS mode permits the exerciser to write information into all bit positions once, until the memory is filled, and then allows the information to be consecutively read out a preset number of times.

The simplest information pattern that can be checked is all 1's or all 0's. Also the information can be varied so that each bit contains the opposite information from the preceding bit, which will produce a 1-0 test pattern either down each word line, down each bit line (plated wire), or down both word and bit lines to produce a checkerboard pattern throughout the memory plane.

6-4. WORST-CASE TEST PATTERNS

The memory exerciser is capable of generating several information patterns. These patterns have been designed with worst-case plated-wire tests in mind.

One test is designed to ensure the nondestructive readout property of the plated wire. This test is implemented by writing into the memory certain information patterns and then repeatedly reading the memory without rewriting. This test is also implemented in combination with other tests.

Another test is to check adjacent-bit disturb. The plated wire, being a continuous-storage medium, is susceptible to adjacent-bit-disturb phenomenon. This is tested by writing 1's once into alternate bits in the memory, and then writing 0's repeatedly into all other bits. The 1's are then read out and checked. This information is then complemented, the 0's read out and checked, and then the roles of the disturbing bits and test bits are reversed and the test procedure is repeated. An added feature of this test allows reading the test bits repeatedly while writing into the disturbing bits. This procedure then checks NDRO as well as adjacent-bit-disturb effects.

As described in Appendix A, the plated wire is subject to disturbing due to adjacent-wire coupling. This effect is tested by writing into adjacent wires the same information as that stored in the bit under test. The information in the bit under test is then read out. Next, information opposite to that stored in the bit under test is written into the adjacent wires, and again the bit under test is read out. This last test is also used to check the diminution of the output signal from the test bit, as seen by the sense amplifier, by the information of opposite polarity stored in the adjacent wires feeding through the off-impedance of nonselected bit-sense matrix switches.

SECTION VII

TEST RESULTS

Final testing of the memory on 31 October, 1966, demonstrated the feasibility of the 10^7-bit plated-wire memory module. Approximately 10^5 -bits, located in the four corners of the plane, were tested. Thus the four limiting physical locations of the bits were investigated.

The only problem which prevented a completely successful worst-case testing arose from irregularities in the memory plane construction. These irregularities produced bumps on the surface of the plane, thus allowing uneven spacing between the word lines and the bit lines and/or the mu-metal keeper and the word lines. This problem was noted during the construction of the plane, and was due to word lines and keeper being put on the plane in a "wallpaper-hanging" fashion. Because of the size of the plane (4 feet by 5 feet), it was not possible to press a plane of this size in a hydraulic press available to us.

Evidence of these irregularities were noted in the electrical testing, as some areas of the plane did not work well electrically.

During initial debugging, system noise was reduced to ±1 millivolt which is a reasonable value.

If the areas with irregularities are neglected, the remaining portion of the plane worked excellently. The good areas operated with a ±5 percent margin on the bit and word currents.

In the easier-pattern test (see heading 6-3) with 128 wires tested in two bit-groups, 99 percent of the wires operated with more than 90 percent good bits.

When the worst-pattern test , (see heading 6-4), was run on these same bits, 20 wires operated with 100 percent good bits while 90 wires operated with more than 95 percent good bits.

Because of a time limitation thorough testing and debugging was not done on bit-groups 3 and 4. However, in preliminary tests it was noted that these bits worked generally as well as the other bit groups. The fact that all bits did not work is attributed to the following reasons:

1. Even in "good" areas of the plane there are some mechanical irregularities. As mentioned previously, the mechanical irregularities are due to the large size of the plane with the accompanying inability to press such a plane.

2. The original wires had occasional bad bits along their length. This point is not fundamental

SECTION VIII

CONCLUSIONS AND RECOMMENDATIONS

A 10^7-bit-position memory plane has been built and populated with 2.3 x 10^6 bits of plated wire, 131,000 of which were exercised. The mechanical configuration of this plane allows for the modular construction of a 10^8-bit mass random access memory with a volume of 20 cubic feet. The full memory would be composed of ten 10^7-bit memory modules.

The module is composed of two planes, each approximately 4 feet by 5 feet by 1/4 inch in size. Mounted on these planes are 2100 6-foot-long word lines and 5000 8-foot-long sense lines. A mu-metal shield, or keeper, covers all the word lines. There is space for mounting the bit-sense-matrix circuits, word line diodes, and A- and B-switch circuits on the planes.

Because of the physical size of the planes, the techniques used for bonding the tunnel structure and the word lines were restricted to hand-rolling and room-temperature-curing adhesives. Electrical connections to the word lines and plated wires were made by soldering.

The design of the plane was such that there would be a total of 15,000 individual plated-wire solder connections and 5000 plated-wire ground connections for each 10^7-bit module, were the entire module to be populated.

After the module was built and operated, several improvements in future design became apparent. One area of improvement is the size. The large physical size of the module makes it difficult to maintain consistent spacings between the base support and the tunnel structure, the tunnel structure and the word lines, and the word lines and mu-metal shield. Other disadvantages arising from the large size are the difficulty in using standard laminating and pressing techniques and the difficulty in the physical handling of the memory and the plated wire because of the awkward form factor.

To improve the mechanical design of the memory plane it is proposed that the 10^7-bit module be composed of smaller memory planes about 3 feet by 3 feet in outside dimensions. Thickness could be reduced from 0.25 inch to 0.125 inch. Such a plane would contain 1000 3-foot-long word lines and 2500 4-foot-long sense lines. Four planes would make up a 10^7-bit module housing 4000 word lines (3 feet long) and 2500 sense lines (16 feet long). Bit-sense-matrix circuits would be mounted on a fifth plane; A- and B-switch components could be mounted on each plane. The dimensions of a 10^7-bit module would be approximately 3 feet by 3 feet by 1.5 inches. The form factor for a 10^8-bit memory would be approximately 3 feet by 3 feet by 1.25 feet, or 12 cubic feet. Allowing space for power supplies and for some circuits not mounted on these planes, the overall volume would be about 3 feet by 3 feet by 2 feet or 18 cubic feet.

There would be a 2:1 increase in the number of solder joints, but the total number of these would be only 30,000, which is not large for a module of this size. The increase in the physical and electrical length of the bit/sense line is reasonable. The use of the smaller plane size would result in easier and better control of the memory construction. Standard pressing equipment used in laminating the planes would permit the close control of plane thickness.

APPENDIX

MEMORY PLANE CONFIGURATION

A-1. EXPERIMENTS TO DETERMINE WORD-LINE CONFIGURATION

A-1.1. EQUIPMENT USED AND PARAMETERS MONITORED

The UNIVAC Plated-Wire Universal Tester (UPWUT) (see Figure 27) was used to measure various plated-wire parameters for different word-line configurations. The UPWUT consists of five high-current drivers (word current drivers), four low-current drivers (bit current drivers), and various control circuitry. Jigs containing different word-line configurations are connected to the current drivers. Current amplitudes and plated-wire outputs are monitored by oscilloscopes. The pulse program of UPWUT is divided into five parts; each one can operate independently, or in any combination of the others. These are:

Part 1 - History: 0's are written in the bit under test, and the right and left adjacent bits.

Part 2 - Single Write: 1 is written into bit under test once.

Part 3 - Adjacent Bit Disturb. The adjacent bits are exercised by writing 0's.

Part 4 - Nondestructive Readout. Bit under test is read out many times.

Part 5 - Readout. Bit under test is read out twice.

The above program is for a 1 test; the opposite information is written into the plated wire for a 0 test. History, ABD, and NDRO can be repeated up to 10,000 times. The current-generation can be adjusted to give worst-case tolerances in the program. The write scheme used is the phase-modulated write.

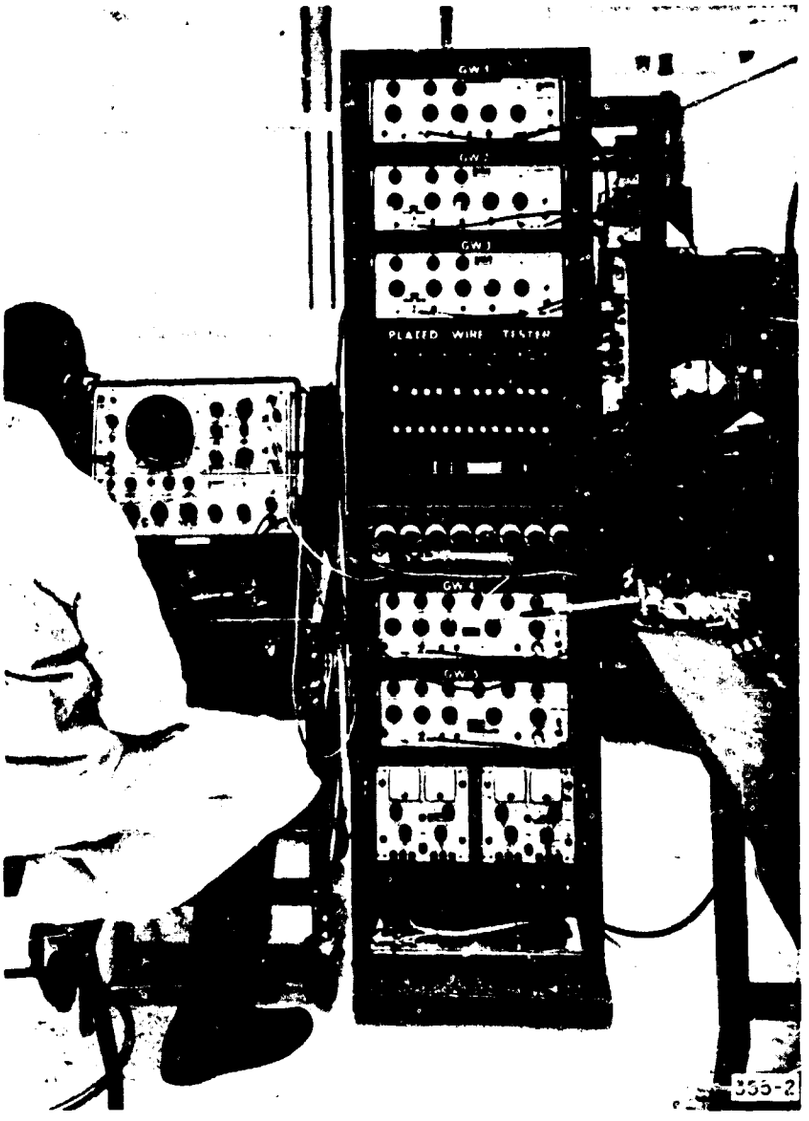


Figure 27. The UNIVAC Plated-Wire Universal Tester

The following jigs are used in the experiments for this project:

EP1 - contains groups of one-turn copper word lines on 0.045-inch centers. The word lines are 0.025 inch, 0.030 inch and 0.035 inch wide.

EP3 - contains both copper word lines and mu-metal-plated-copper word lines on 0.045-inch centers using aluminum as the ground return. These are called half-turn word lines, and are 0.015 inch to 0.040 inch wide.

The parameters that were monitored are shown in Table III.

A-1.2. RESULTS

Figures 28, 29, and 30 show I_{wP}, I_{wD}, I_{wA} and E_o as functions of width of word lines. Curves in Figure 28 are for EP1 (one-turn copper word lines). Those in Figure 29 are for EP3 (half-turn mu-metal-copper word lines), while those in Figure 30 are for EP3 (half-turn copper word lines with a mu-metal keeper, 1-mil shield-mu 30 from Magnetic Metals, Camden, N. J., 0.004 inch away from the word lines). The curves indicate that the keeper has the following effects:

The mu-metal reduces I_{wA}, or the effect of adjacent-bit spreading, and also reduces the word-current requirement.

The mu-metal also reduces the dependence of word-current requirement on word-line width.

Putting a sheet of mu-metal on top of the word lines is almost as effective as making a combination mu-metal-copper word line.

Figure 31 shows I_{wP} and I_{wD} for half-turn mu-metal-copper word lines as functions of the number of pairs of plated wire inserted next to the test wire. The results show that the current increases as the number of wires is increased.

Figure 32 shows E_o and switching time as functions of the word-current rise time. Results are for 0.035-inch and 0.025-inch half-turn mu-metal copper word lines. Different plated wires are used for the two sets of word lines. E_o and switching times are fairly linear functions of word-current rise time. Figure 33 shows I_{wP} and I_{wD} for half-turn copper word lines with mu-metal keepers as functions of separation of the word lines and the mu-metal sheet. For close separation, I_{wP} and I_{wD} vary about 2 percent per 0.001 inch of separation. Based on the above results, the decision has been made to use half-turn copper word line with mu-metal keeper.

Table III. Parameters Monitored in Plated-Wire Test

Parameters Monitored	HISTORY Adverse Information Written into Left and Right Adjacent Bits and Test Bit 250 Times	SINGLE WRITE Desired Information Written into Test Bit Once	ADJACENT BIT DISTURB Adverse Information Written into Left and Right Adjacent Bits 2500 Times	NDRO Read Out Test Bit 250 Times	RO Read Out Test Bit 2 Times
I_{wP}	Nonoperative	$I_b = \pm 33$ ma	Nonoperative	Nonoperative	*
I_{wD}	Nonoperative	$I_b = \pm 33$ ma	Nonoperative	I_w is increased until the plated wire output is decreased by 25%. This value of I_w is I_{wD}.	$I_w = I_{wP} + 15\%$
I_{wA}	Operative only on right adjacent bit and bit under test. $I_w = \frac{I_{wP} + I_{wD}}{2} = I_N$ $I_b = \pm 35$ ma ± 2 ma	$I_b = \pm 35$ ma ± 2 ma $I_w = I_N$	$I_b = \pm 33$ ma ± 2 ma On left adjacent bit I_w is increased until the plated wire output is decreased by 25%. This I_w is I_{wA}.	$I_w = I_N$	$I_w = I_N$
E_o	$I_w = \frac{I_{wP} + I_{wD}}{2} + 5\%$ $= I_N + 5\%$ $I_b = \pm 35$ ma ± 2 ma	$I_b = \pm 35$ ma ± 2 ma $I_w = I_N - 5\%$	$I_w = I_N + 5\%$ $I_b = \pm 33$ ma ± 2 ma	$I_w = I_N + 5\%$	Peak-to-peak output of plated wire is E_o. $I_w = I_N - 5\%$

*I_w for single write and readout operations is increased from low value until the plated wire shows positive and negative outputs. This value of I_w is I_{wP}. The appearance of the positive and negative outputs is sudden and the current at which they appear is well defined.

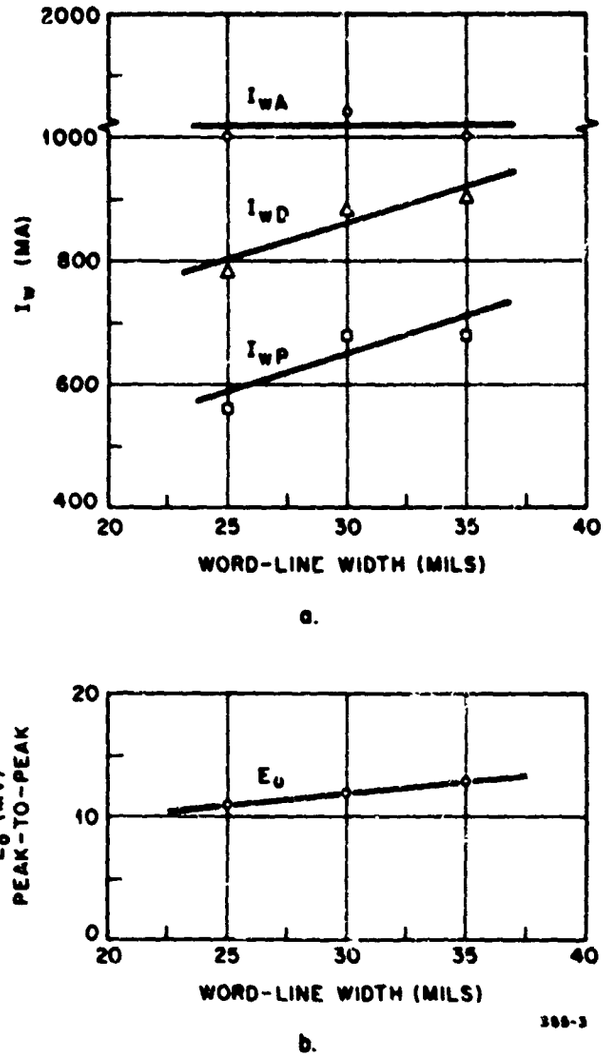


Figure 28. Word Current (a) and Output (b) as Functions of Line Width, for One-Turn Copper Word Lines

The half-turn is favored over the one-turn configuration because the requirement to register the top half with the bottom half of the one-turn line is eliminated. Ease of mechanical fabrication is also the reason for choosing the copper lines with mu-metal backing rather than the mu-metal-copper lines. The word lines will be 0.033 ± 0.002 inch wide on 0.045 ± 0.003-inch centers. The accumulative tolerance of the word-line centers is ±0.005 inch for a given word strap. The nominal current is expected to be about 800 milliamperes, and the nominal bit current will be ±35 milliamperes. The nominal output for ±5 percent current worst-case variation will be 10 millivolt peak-to-peak.

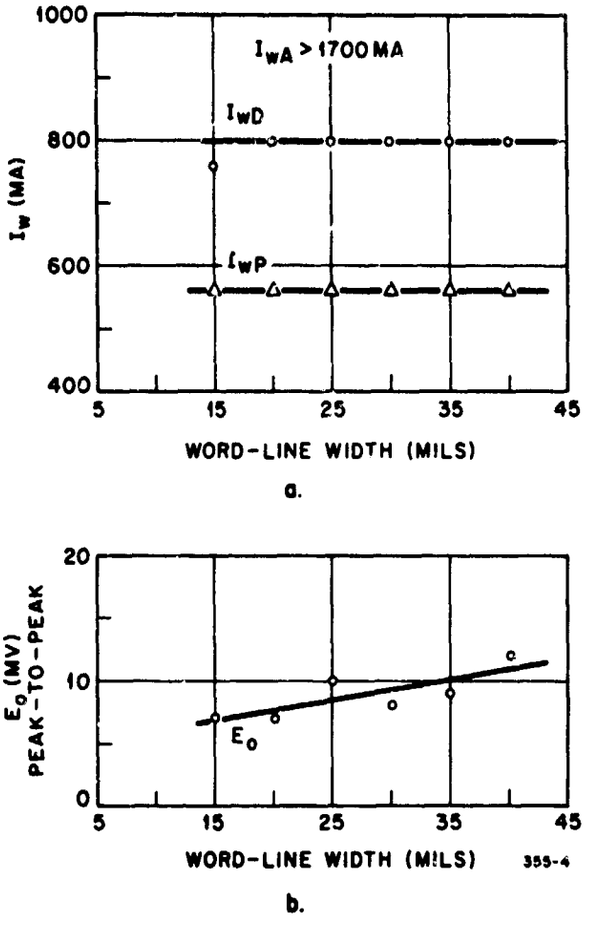
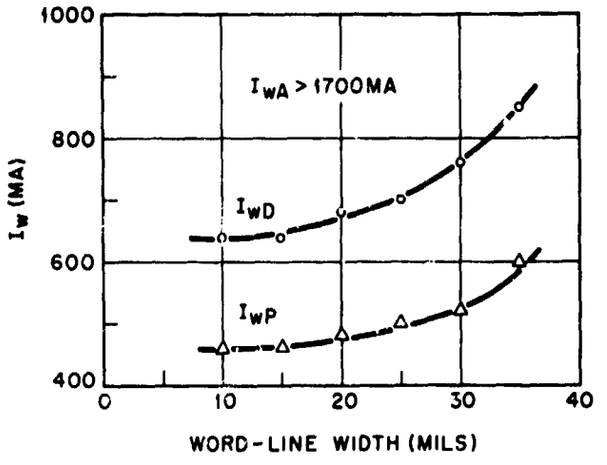


Figure 29. Word Current (a) and Output (b) as Functions of Line Width, for Half-Turn Mu-Metal-Copper Word Lines

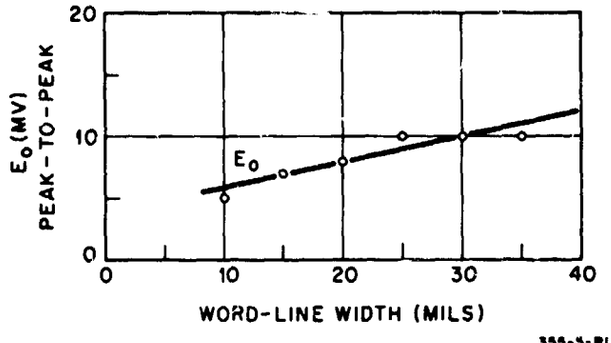
A-2. ADJACENT-WIRE COUPLING

Adjacent-wire coupling is the phenomenon whereby a fraction of the signal appearing on one plated wire is coupled into adjacent wires. It is caused by the mutual impedance between a pair of closely spaced plated wires. When the current pulse is applied to a word line during a read instruction, signals are generated in all wires passing under that word line. Signals generated in wires adjacent to those being sensed will couple unwanted voltages into the sensed wires. It is important that the nature and extent of this coupling be understood for a memory of this size.

The experimental technique used to measure the adjacent-wire coupling has been designed to make the observations meaningful and accurate. Since it is impractical to construct a full-size memory plane of every type of construction under consideration, small test planes are used. These have a



a.



b.

Figure 30. Word Current (a) and Output (b) as Functions of Line Width, for Half-Turn Copper Word Lines with Mu-Metal Keepers

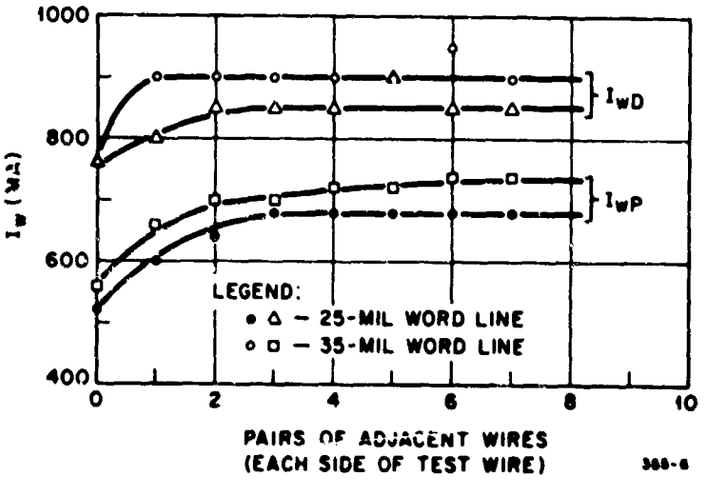


Figure 31. Word Current as Function of Number of Adjacent Wires

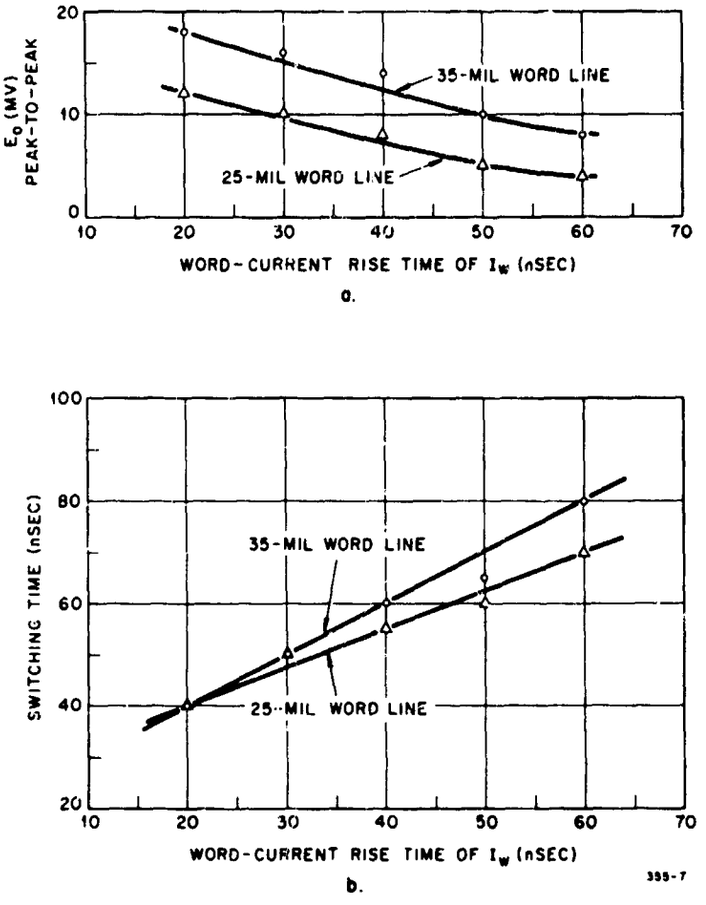


Figure 32. E_0 (a) and Switching Time (b) as Functions of Word-Current Rise Time

group of 1-foot-long word lines bonded over a plated-wire carrier with tunnels for plated wires on 0.015-inch centers. The entire assembly is bonded to a ground plane. It is possible to simulate a long length of plated wire by a series connection of shorter lengths. Ten feet of plated wire are evenly spaced throughout the test plane and connected in this fashion. Similar 10-foot lengths are placed in grooves adjacent to the first one. One end of each 10-foot run is grounded, and the other is terminated in the characteristic impedance of the wire, about 50 ohms.

Coupling is measured by injecting a signal into one of the 10-foot wires and viewing the resultant signal in an adjacent wire either 15 or 30 mils

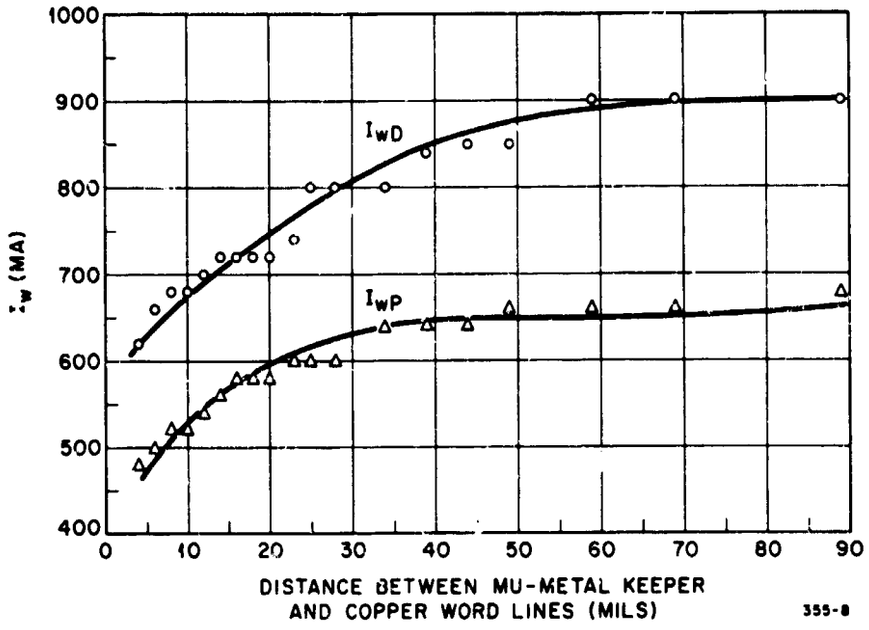


Figure 33. Word Current as Function of Separation of Word Lines from Mu-Metal Keeper

away. Injecting a signal is accomplished in the following manner. The 10-foot wire is broken at a point and an additional 2-inch length inserted in series with it. This short length is located on a small fixture about 2 ½ inches square, and is crossed by several 1-inch-long word lines. Writing on this short segment is accomplished by passing through it a d-c current whose amplitude exceeds the H_c of the wire. It is read out by driving word current down one of the short word lines. The readout signal then travels down the 10-foot plated wire following transmission-line laws, and the coupled signal is viewed in the adjacent wire.

System noise is minimized by using a differential amplifier whose dummy input is another 10-foot length of wire running through the test plane about 0.2 inch from the wire being sensed. Noise is thus reduced to well below 1 millivolt peak-to-peak.

The signal delay through 10 feet of plated wire is about 30 nanoseconds. This means that there is a significant difference between a signal generated at the sense amplifier end of the line and one generated at the grounded end. For this reason, adjacent-wire coupling is checked at both ends of the wire and in the middle. The wire was terminated in the characteristic impedance at the sense amplifier. While a higher resistance might be used in the final

memory system to raise the sense signal amplitude, it is believed that characteristic impedance termination represented the most general case.

Waveforms are shown in Figure 34 for a test plane of the construction

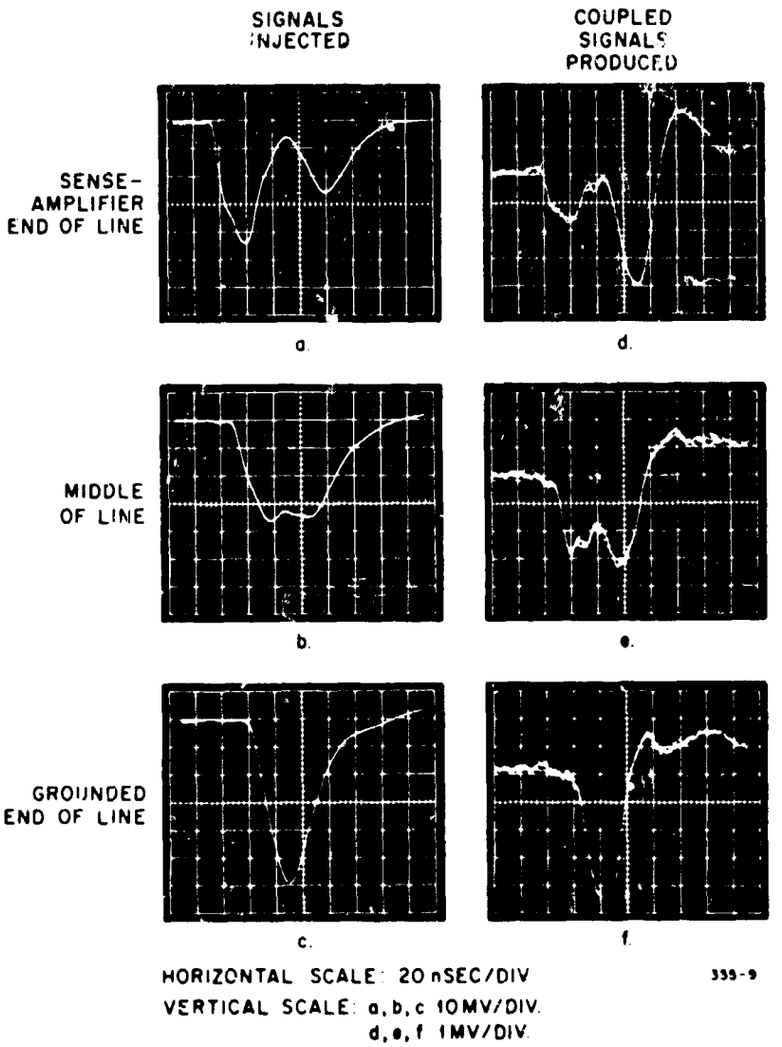


Figure 34. Waveforms Showing Adjacent-Wire Coupling, Viewed from Sense Amplifier End of Line

contemplated for the final system. Word lines are 0.33 inch wide, on 0.045-inch centers. A magnetic keeper is placed 0.004 inch above the word lines. Only one polarity of output signal is shown; the other polarity gives similar waveforms. They are shown for signals injected at the terminated (sense amplifier) end of the line, in the middle of the line, and at the grounded end. The first group (Figures 34a, b, c) are waveforms of the signal seen at the terminated end of the wire in which the signal is injected. Since

the sense amplifier used was linear but its exact gain was not measured, the output amplitudes shown are all relative.

From these waveforms several points, all related to the transmission-line nature of the plated wire over a ground plane, should be noted. When a signal is injected at the grounded end of the wire, the sense amplifier sees a single signal. But when the signal is injected near the amplifier, there is an initial signal and then a delayed one caused by the reflection at the grounded end. The area under each output is essentially constant, however. This fact suggests the use of a sense amplifier which integrates the signal, rather than one which merely detects the peaks. In this manner, full use is made of the output signal regardless of shape.

Examination of the coupled signal (Figures 34d, e, f) provides a further reason for using an integrating sense amplifier. The coupled signal swings to both sides of ground. Thus, by integrating this signal, the effect is minimized. Data has been taken of coupling for wires on 0.030-inch centers, and it appears to be very close to half that of wires on 0.015-inch centers.

Table IV indicates the percentage of coupling into a wire 0.015 inches away for three points of signal injection. The figure given represents the ratio of the highest peak of the coupled signal to the highest peak of the injected signal, viewed at the terminated end of the wire. Comparative data is also given for the same plane without the magnetic keeper.

Work is scheduled for the near future to develop a greater understanding of the nature of adjacent-wire coupling.

Table IV. Percentage of Coupling, 0.015-inch Wire Spacing

Point of Signal Injection	Coupling Percentage	
	20 ns*	35 ns*
With Magnetic Keeper:		
Terminated end	9.3	8.9
Middle of line	8.9	8.8
Grounded end	7.8	8.0
Without Magnetic Keeper:		
Terminated end	7.6	7.3
Middle of line	7.6	6.6
Grounded end	10.0	9.0

*Word-current rise time.

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13. ABSTRACT

The concept of a nonmechanical, mass, random access, plated-wire memory has been validated in this phase of the continuing U.S. Air Force program. The memory model fabricated for this contract has 10^7-bit positions housing over 2.3 megabits of plated wire. Of these bits, 32,768 4-bit words have been exercised with a memory exerciser. The following characteristics of the plated-wire mass memory have been demonstrated.

Nondestructive readout (NDRO),
Selection in the bit dimension to minimize electronics costs,
Simple mechanical plane configuration,
Random access,
Electrical alterability.

The final test of the plane revealed some defective areas which resulted from the large surface area. Making a smaller plane would easily eliminate this condition.

All the objectives of the program have been achieved, including the projected production cost of less than $0.01 per bit. The contractor feels that as a result of this program, the building of a mass (10^6-bit), random access, plated-wire memory is economically feasible and well within the state-of-the-art.

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